1. General Description

The family of WP1507 is a highly integrated e-Fuse protection IC. It has multiple protection modes including current limiting, overvoltage clamping, short circuit protection and over-temperature protection.

Current limit threshold is programmed with a resistor from ILIM to ground. The devices provide over voltage protection (OVP) for 5/12V systems. Over voltage protection are limited by internal clamping circuits to a safe fixed maximum, with no external components required. The soft-start time is set with a capacitor from the dV/dT pin to the ground to limit the current surge during start-up. The device is available in a Green DFN-3x3-10L packages.

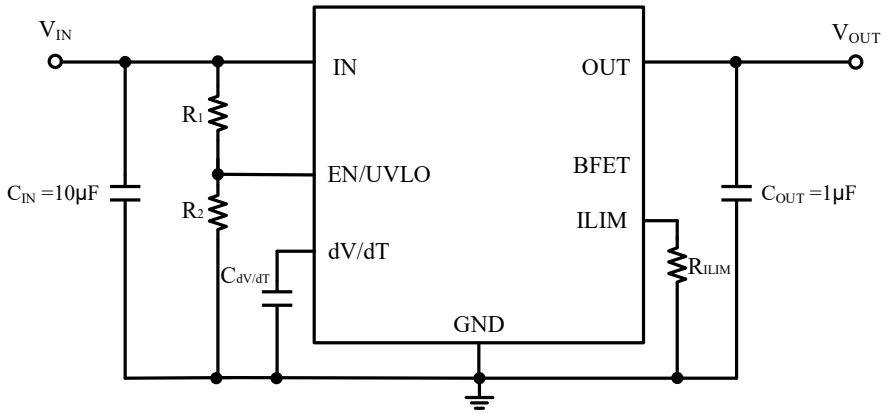
2. Features

- Input Voltage Range: 4.5 V to 18 V
- Typical $R_{DS(ON)}$: 28mΩ N-Channel
- Adjustable Current Limit: 1A~5A
- Fixed Over-Voltage Clamp：6.1V/15V
- Programmable V_{OUT} Slew Rate
- Reverse Current Blocking Support
- Built-in Thermal Shutdown
- UL2367 certification in process
- Available in Green DFN-3×3-10L Package

3. Applications

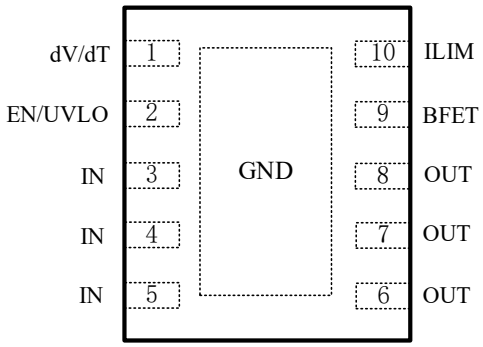
- HHD and SSD Drives
- Set Top Boxes
- Servers and AUX Supplies
- PCI and PCIe Cards
- Adapter Powered Devices
- USB Power Distribution
- USB Protection
- USB 3.1 Power Delivery

4. Typical Application



NOTE: This electric circuit only supplies for reference.

5. Pin Configuration



TOP VIEW
DFN 3× 3-10L

6. Pin Description

PIN NUMBER	PIN NAME	I/O	PIN FUNCTION
1	dV/dT	O	Connect a capacitor from this pin to GND to control the ramp rate of OUT voltage at device turn on.
2	EN/UVLO	I	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal MOSFET. When pulled high, it enables the device. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
3,4,5	IN	I	Power Input Pin.
6,7,8	OUT	O	Power Output Pin.
9	BFET	O	Connect this pin to the gate of a blocking NFET.
10	ILIM	O	A resistor from this pin to GND sets the overload and short circuit limit.
Thermal Pad	GND	Ground	GND.

7. Production Modes

PART NUMBER	OVP CLAMP	FAULT RESPONSE
WP1507-AFEAR	-	Latched
WP1507-BFEAR	-	Auto Retry
WP1507-CFEAR	6.1V	Latched
WP1507-DFEAR	6.1V	Auto Retry
WP1507-EFEAR	15V	Latched
WP1507-FFEAR	15V	Auto Retry

8. Absolute Maximum Ratings [1]

T_A=25℃, unless otherwise noted.

SYMBOL	PARAMETER	RATING	UNIT
IN	Input Voltage	-0.3 to 20	V
OUT	OUT Voltage	-0.3 to V_{IN} + 0.3	V
ILIM	Voltage	-0.3 to 7	V
EN/UVLO		-0.3 to 7	V
dV/dT		-0.3 to 7	V
BFET		-0.3 to 30	V
T_{STG}	Storage Temperature	-65 to 150	℃
T_{SDR}	Lead Temperature (Soldering, 10 sec)	260	℃
ESD	Human Body Model	2	kV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
IN	Input Voltage	4.5	-	18	V
BEFT		0	-	V_{IN} + 6	V
dV/dT, EN/UVLO		0	-	6	V
ILIM		0	-	3	V
I_{OUT}	Continuous output current	0	-	5	A
R_{ILIM}	Resistance	10	100	162	kΩ
C_{OUT}	External capacitance	0.1	1	1000	μF
$C_{dV/dT}$			1	1000	nF
T_A	Operating Ambient Temperature	-40	25	85	℃
T_J	Operating Junction Temperature	-40	25	125	℃

10. Electrical Characteristics

(V_{IN} = 12 V for WP1507-A/B/E/F, V_{IN} = 5V for WP1507-C/D, $V_{EN/UVLO}$ = 2 V, C_{IN} = 10μF, C_{OUT} = 1μF, $C_{dV/dT}$ = OPEN, T_A=25℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
IN (INPUT SUPPLY)							
V_{UVLO}	Input UVLO Threshold, Rising	Enabled, V_{IN} rising		4.15	4.3	4.45	V
V_{UVLO_HYS}	Input UVLO Hysteresis [2]				0.2		V
I_Q	Quiescent current	Enabled: EN/UVLO = 2 V	WP1507-A/B/E/F	300	420	550	μA
			WP1507-C/D	350	470	600	μA
I_{SHDN}	Shutdown Current	Disabled: EN/UVLO = 0 V			130	225	μA
V_{OVC}	Over-voltage clamp	WP1507-C/D V_{IN}>6.75V, I_{OUT}=10mA		5.25	6.1	6.75	V
		WP1507-E/F V_{IN}>16.5V, I_{OUT}=10mA		13.8	15	16.5	V
EN/UVLO (ENABLE/UVLO INPUT)							
V_{ENH}	EN threshold voltage, rising			1.37	1.40	1.44	V
V_{ENL}	EN threshold voltage, falling			1.32	1.35	1.39	V
I_{EN}	EN input leakage current	0V ≤ V_{EN} ≤5V		-0.1	0	0.1	μA
dV/dT (OUTPUT RAMP CONTROL)							
$I_{dV/dT}$	dV/dT charging current [2]	$V_{dV/dT}$ = 0 V			220		nA
R_{dV/dT_disch}	dV/dT discharging resistance	$V_{EN/UVLO}$ = 0 V, $I_{dV/dT}$ = 10 mA sinking		50	73	100	Ω
$V_{dV/dTmax}$	dV/dT maximum capacitor voltage [2]				5.5		V
$GAIN_{dV/dT}$	dV/dT to OUT gain [2]	$\triangle V_{dV/dT}$			4.85		V/V
ILIM (CURRENT LIMIT PROGRAMMING)							
I_{LIM}	I_{LIM} bias current [2]				10		μA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Overload current limit	R_{ILIM} = 10 kΩ, V_{IN-OUT} = 1 V		1.02		A
		R_{ILIM} = 45.3 kΩ, V_{IN-OUT} = 1 V	1.79	2.1	2.42	A
		R_{ILIM} = 100 kΩ, V_{IN-OUT} = 1 V	3.46	3.75	4.03	A
		R_{ILIM} = 150 kΩ, V_{IN-OUT} = 1 V	4.5	5.1	5.7	A
$I_{OL-R-Short}$		R_{ILIM} = 0 Ω, shorted resistor current limit		0.84		A
$I_{OL-R-Open}$		R_{ILIM} = OPEN, open resistor current limit		0.80		A
I_{SCL}	Short-circuit current limit	R_{ILIM} = 10kΩ, V_{IN-OUT} = 5 V WP1507-C/D		1.0		A
		R_{ILIM} = 10kΩ, V_{IN-OUT} = 12 V WP1507-A/B/E/F		1.0		A
		R_{ILIM} = 45.3kΩ, $V_{VIN-OUT}$ = 5 V, WP1507-C/D	1.72	2.05	2.42	A
		R_{ILIM} = 45.3kΩ, $V_{VIN-OUT}$ = 12V, WP1507-A/B/E/F	1.66	1.98	2.37	A
		R_{ILIM} = 100kΩ, $V_{VIN-OUT}$ = 5 V, WP1507-C/D	3.1	3.56	4.0	A
		R_{ILIM} = 100kΩ, $V_{VIN-OUT}$ = 12V, WP1507-A/B/E/F	2.9	3.32	3.85	A
		R_{ILIM} = 150kΩ, $V_{VIN-OUT}$ = 5V, WP1507-C/D	4.22	4.95	5.69	A
		R_{ILIM} = 150kΩ, $V_{VIN-OUT}$ = 12V, WP1507-A/B/E/F	3.7	4.5	5.5	A
$RATIO_{FASTRIP}$	Fast-trip comparator level w.r.t.overload current limit [2]	$I_{FASTRIP}$: I_{OL}		160%		
$V_{OpenILIM}$	ILIM open resistor detect threshold [2]	V_{ILIM} Rising, R_{ILIM} = OPEN		3.1		V
OUT (PASS FET OUTPUT)						
t_{ON}	Turn on delay [2]	EN/UVLO→H to I_{IN} = 100 mA, 1A resistive load at OUT		220		μs
$R_{DS(ON)}$	FET ON resistance	T_J =-40℃ to 125℃	21	28	50	mΩ
$I_{OUT-OFF-LKG}$	OUT bias current in off state	$V_{EN/UVLO}$=0V, V_{OUT}=0V (sourcing)	-5	0	1.2	μA
$I_{OUT-OFF-SINK}$		$V_{EN/UVLO}$ = 0V, V_{OUT} = 300 mV (sinking)	10	15	20	

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BFET (BLOCKING FET GATE DRIVER)						
I_{BFET}	BFET charging current [2]	$V_{BFET} = V_{OUT}$		2		µA
$V_{BFETmax}$	BFET clamp voltage [2]			V_{IN} + 5.9		V
$R_{BFETdisch}$	BFET discharging resistance to GND	$V_{EN/UVLO}$ = 0 V, I_{BFET} = 100 mA	15	26	36	Ω
THERMAL SHUT DOWN (TSD)						
T_{SHDN}	TSD threshold, rising [2]			160		°C
$T_{SHDNhyst}$				20		°C
dV/dT (OUTPUT RAMP CONTROL)						
$t_{dV/dT}$	Output ramp time	WP1507-A/B/E/F, EN/UVLO → H to OUT = 11.7V, C_{dVdT} =0	0.7	1	1.3	ms
		WP1507-C/D, EN/UVLO → H to OUT = 4.9V, C_{dVdT} = 0	0.28	0.4	0.52	ms
		WP1507-A/B/E/F, EN/UVLO → H to OUT = 11.7V, C_{dVdT} =1nF		12		ms
		WP1507-C/D, EN/UVLO → H to OUT = 4.9V, C_{dVdT} =1nF		5		ms
ILIM (CURRENT LIMIT PROGRAMMING)						
$t_{FastOffDly}$	Fast-trip comparator delay [2]	$I_{OUT} > I_{FASTRIP}$ to I_{OUT} = 0 (Switch off)		300		ns
BFET (BLOCKING FET GATE DRIVER)						
$t_{BFET-ON}$	WP1507-A/BE/F BFET turn on duration [2]	EN/UVLO → H to V_{BFET} = 12 V, C_{BFET} = 1 nF		4.2		ms
		EN/UVLO → H to V_{BFET} = 12 V, C_{BFET} = 10 nF		42		
$t_{BFET-OFF}$	WP1507-A/B/E/F BFET Turnoff duration [2]	EN/UVLO → L to V_{BFET} = 1 V, C_{BFET} = 1 nF		0.4		µs
		EN/UVLO → L to V_{BFET} = 1 V, C_{BFET} = 10 nF		1.4		
THERMAL SHUTDOWN (TSD)						
t_{TSDdly}	Retry delay after TSD recovery, $T_J < [T_{SHDN} – 20°C]$ [2]	WP1507-B/D/F		300		µs

Note 2: Guaranteed by characterization testing and design.

11. Typical Performance Characteristics

(WP1507-A/B，V_{IN}=12V, $V_{EN/UVLO}$=2V, R_{LIM}=100kΩ, C_{IN}=10μF, C_{OUT}=1μF, $C_{dV/dT}$=open, T_A=25℃, unless otherwise noted)

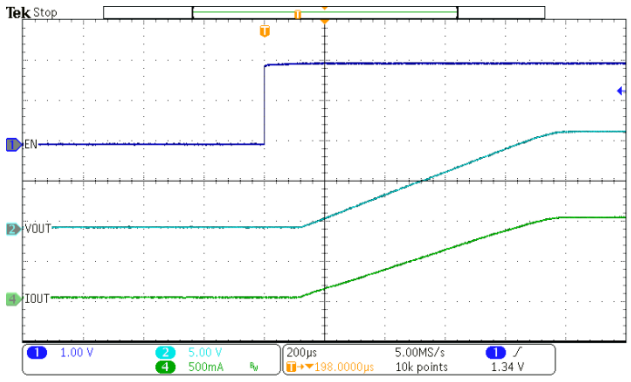


Figure 1. Turn on delay

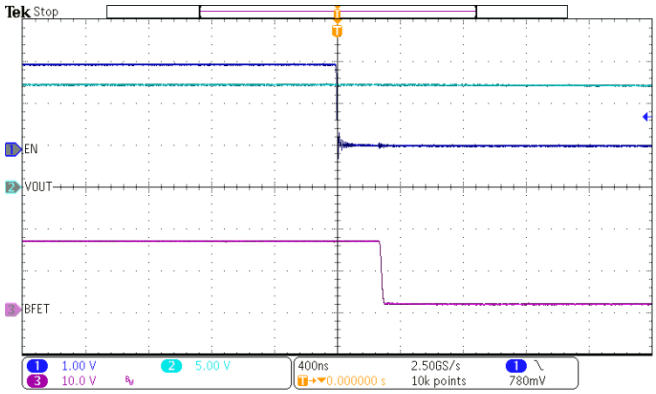


Figure 2. Turn off delay

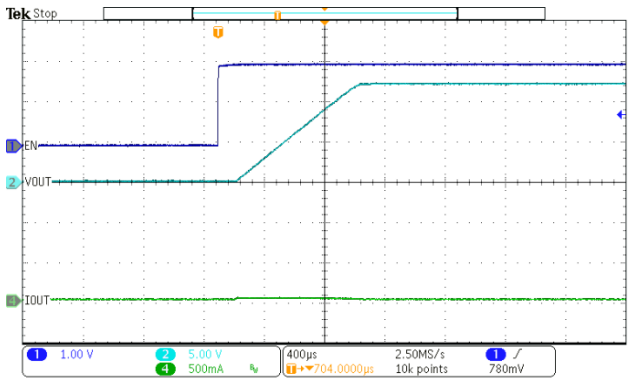


Figure 3. Output ramp time ($C_{dV/dT}$ = 0nF)

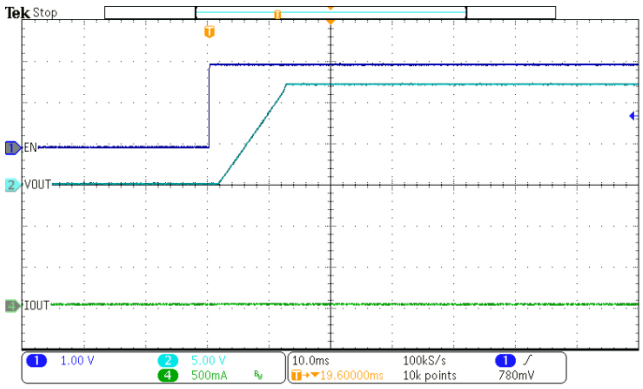


Figure 4. Output ramp time ($C_{dV/dT}$ = 1nF)

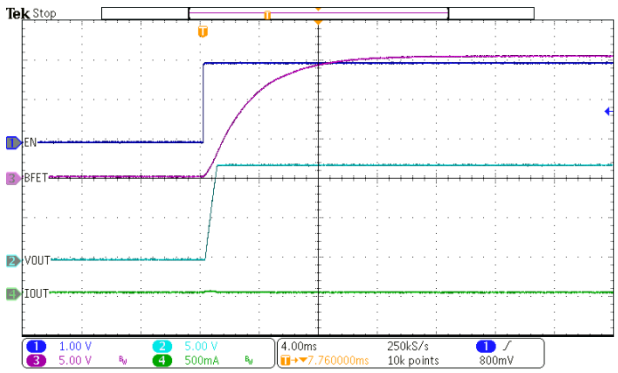


Figure 5. BFET turn on duration (C_{BFET} = 1nF)

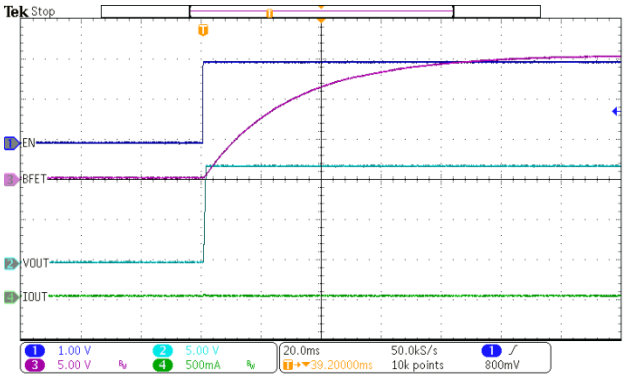


Figure 6. BFET turn on duration (C_{BFET} = 10nF)

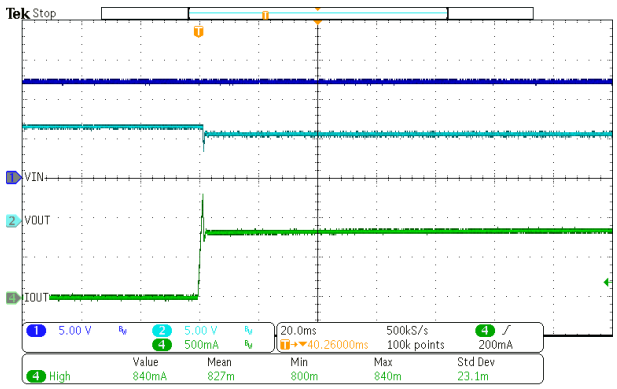


Figure 7. Overload current limit (R_{ILIM} = 0 Ω)

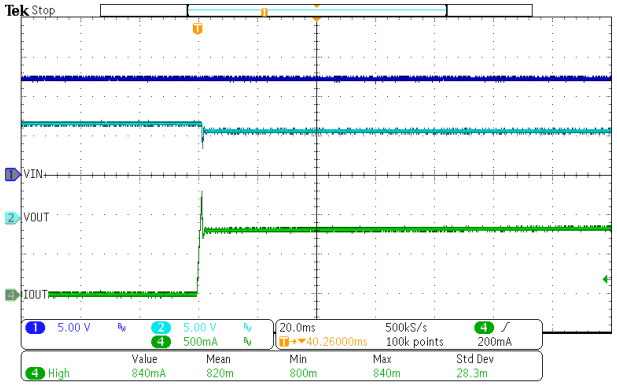


Figure 8. Overload current limit (R_{ILIM} = OPEN)

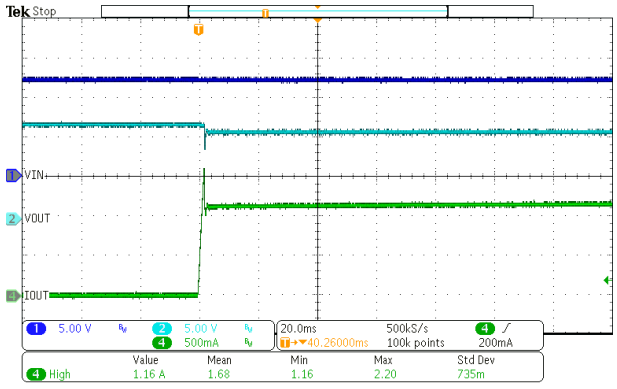


Figure 9. Overload current limit (R_{ILIM} = 10 kΩ)

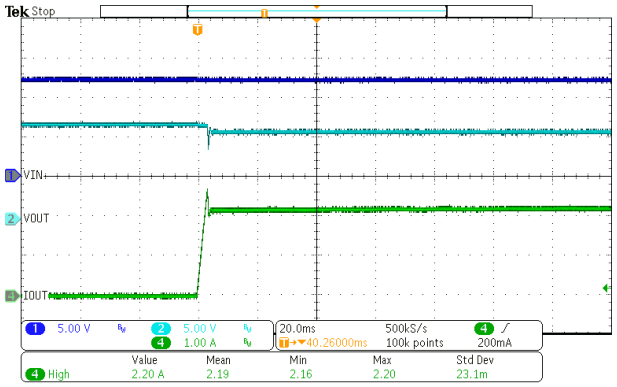


Figure 10. Overload current limit (R_{ILIM} = 45.3 kΩ)

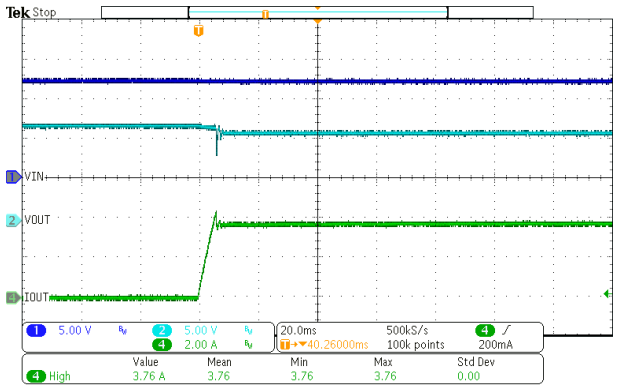


Figure 11. Overload current limit (R_{ILIM} = 100 kΩ)

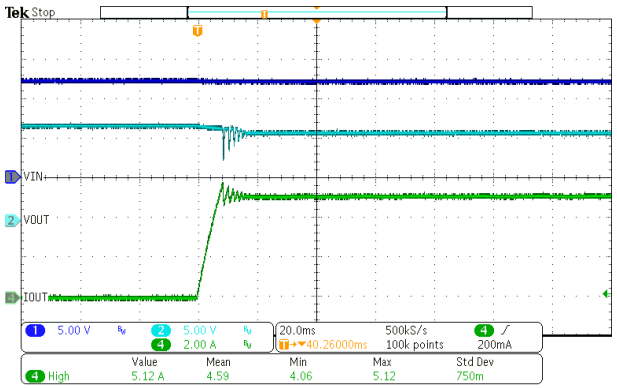


Figure 12 Overload current limit (R_{ILIM} = 150 kΩ)

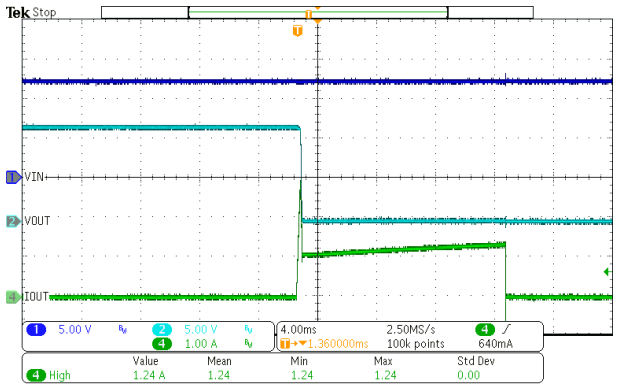


Figure 13 Short-circuit current limit (R_{ILIM} = 10 kΩ)

WP1507-A/B/E/F

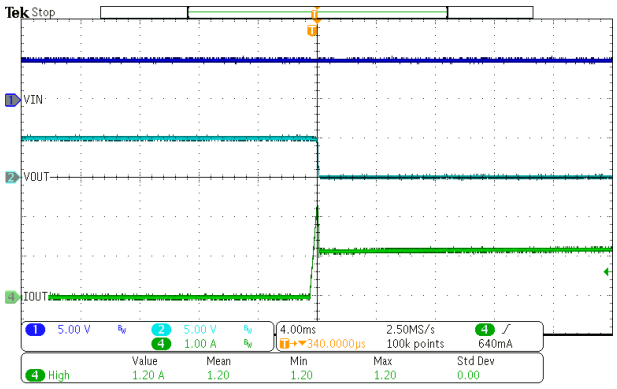


Figure 14 Short-circuit current limit (R_{ILIM} = 10 kΩ)

WP1507-C/D

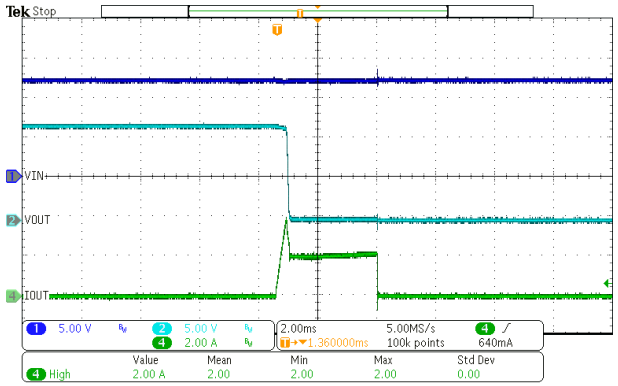


Figure 15 Short-circuit current limit (R_{ILIM} = 45.3 kΩ)

WP1507-A/B/E/F

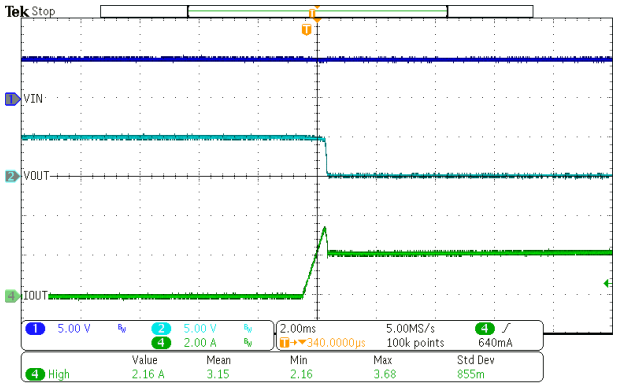


Figure 16 Short-circuit current limit (R_{ILIM} = 45.3 kΩ)

WP1507-C/D

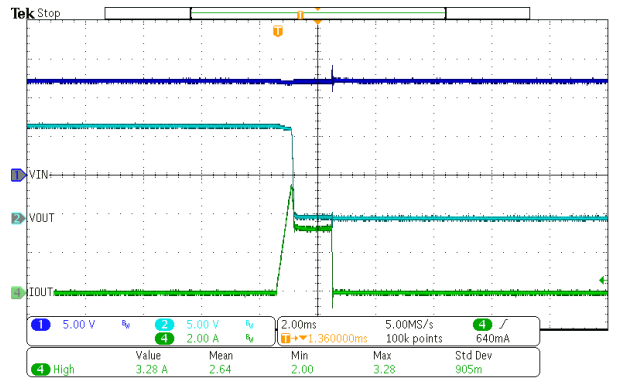


Figure 17 Short-circuit current limit (R_{ILIM} = 100 kΩ)

WP1507-A/B/E/F

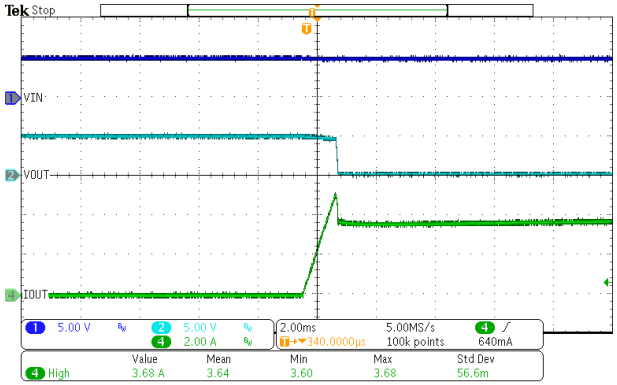


Figure 18 Short-circuit current limit (R_{ILIM} = 100 kΩ)

WP1507-C/D

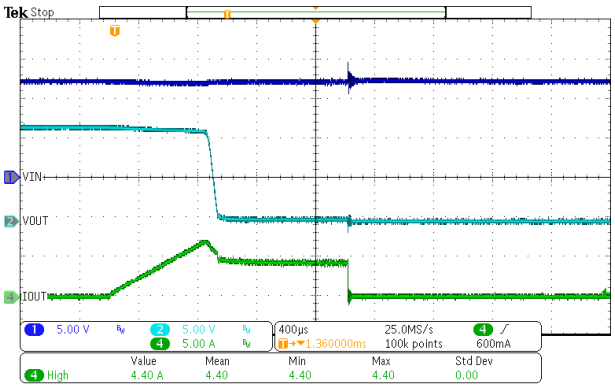


Figure 19 Short-circuit current limit (R_{ILIM} = 150 kΩ) WP1507-A/B/E/F

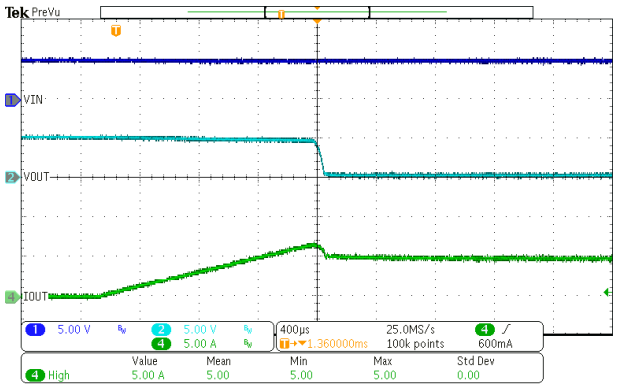


Figure 20 Short-circuit current limit (R_{ILIM} = 150 kΩ) WP1507-C/D

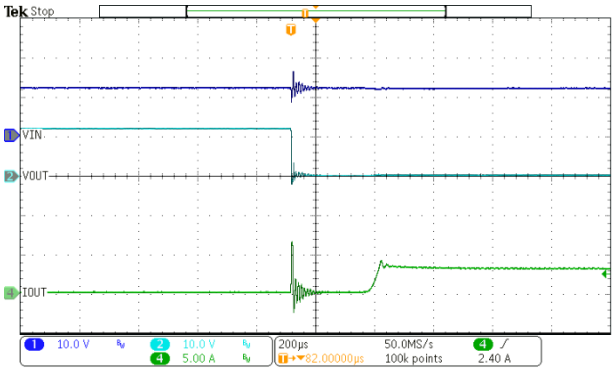


Figure 21 Output Short Circuit

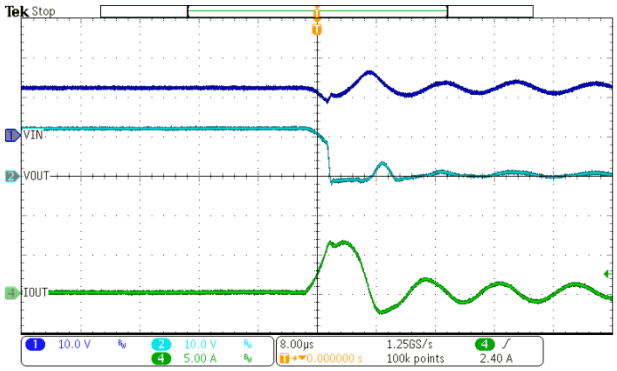


Figure 22 Short Circuit (Zoom) : Fast-Trip Comparator

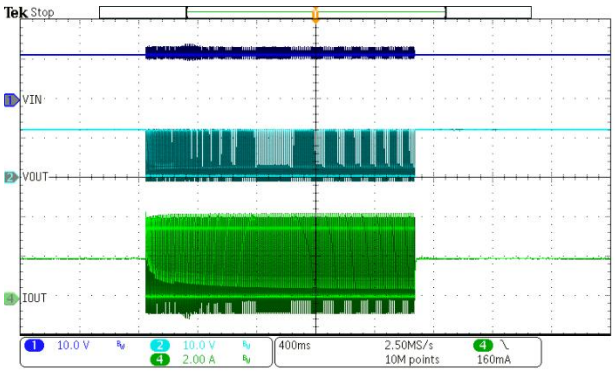


Figure 23 Thermal Fault Auto-Retry

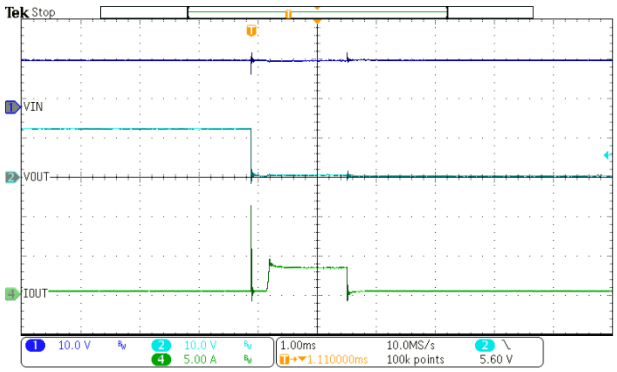


Figure 24 Thermal Fault Latched

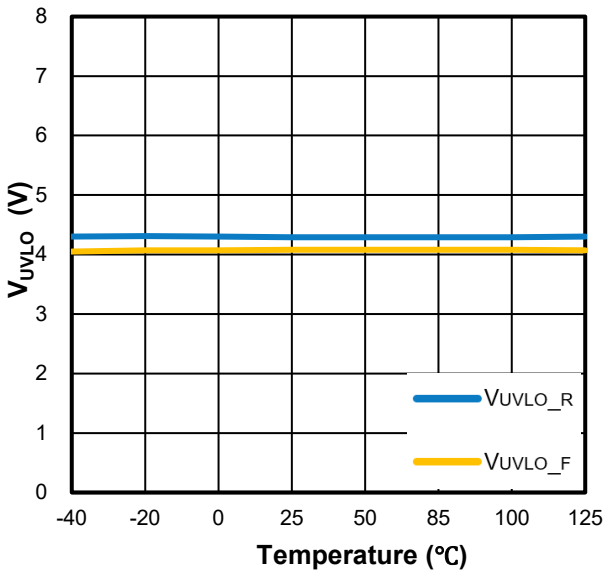


Figure 25. V_{UVLO} vs. Temperature

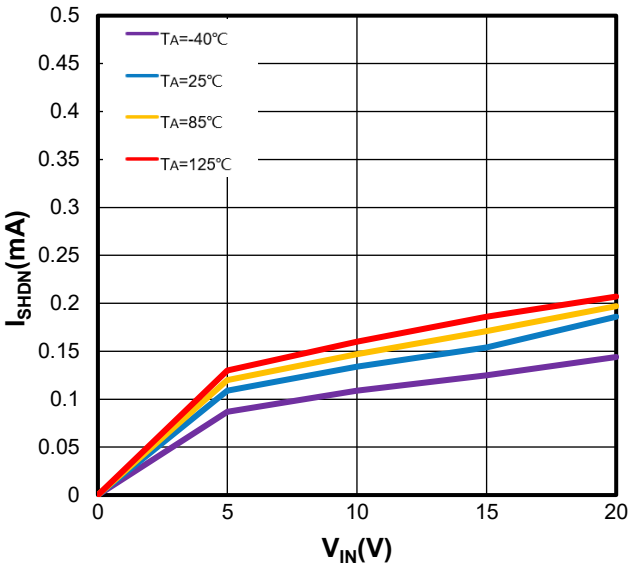


Figure 26. I_{SHDN} vs. V_{IN}

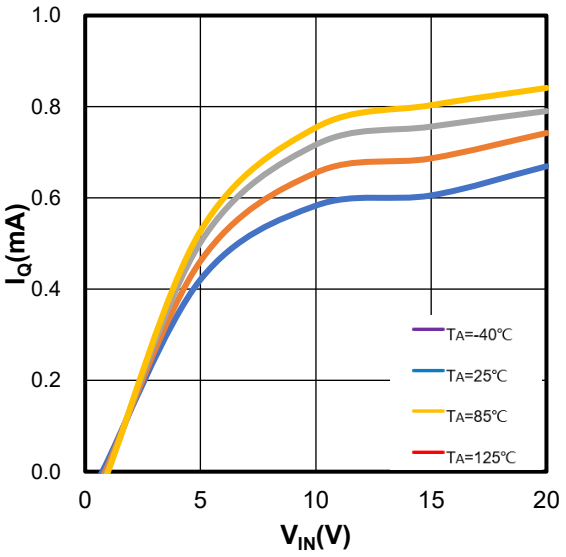


Figure 27. I_Q vs. V_{IN} WP1507-C/D

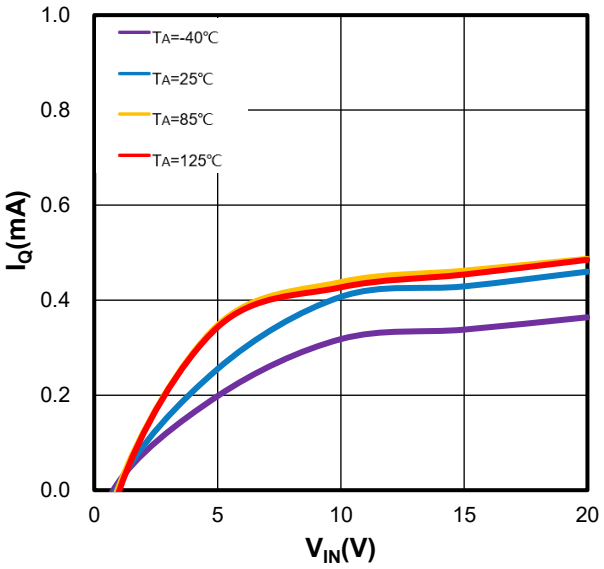


Figure 28. I_Q vs. V_{IN} WP1507-A/B/E/F

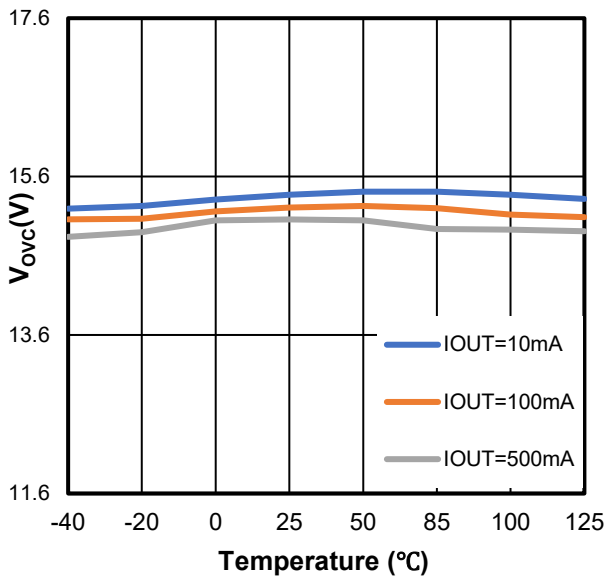


Figure 29. V_{OVC} vs. Temperature Across IOUT

WP1507-E/F

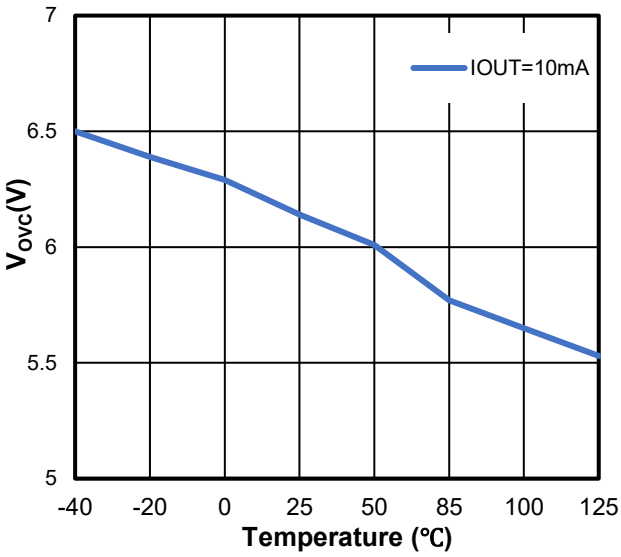


Figure 30. V_{OVC} vs. Temperature

WP1507-C/D

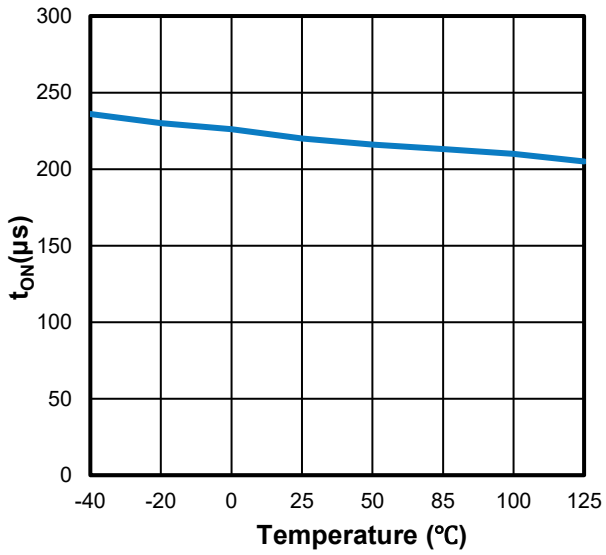


Figure 31. t_{ON} vs. Temperature

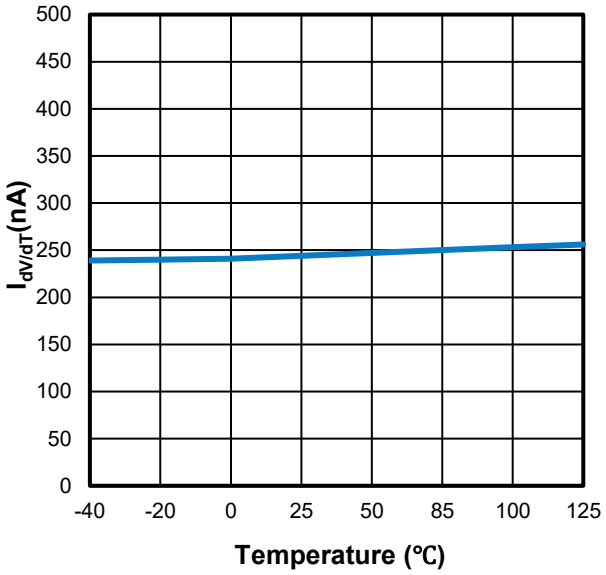


Figure 32. $I_{dV/dT}$ vs. Temperature

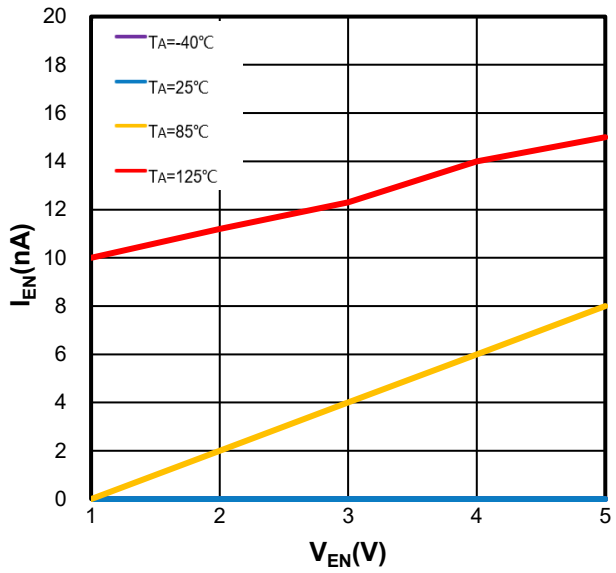


Figure 33. I_{EN} vs. V_{EN}

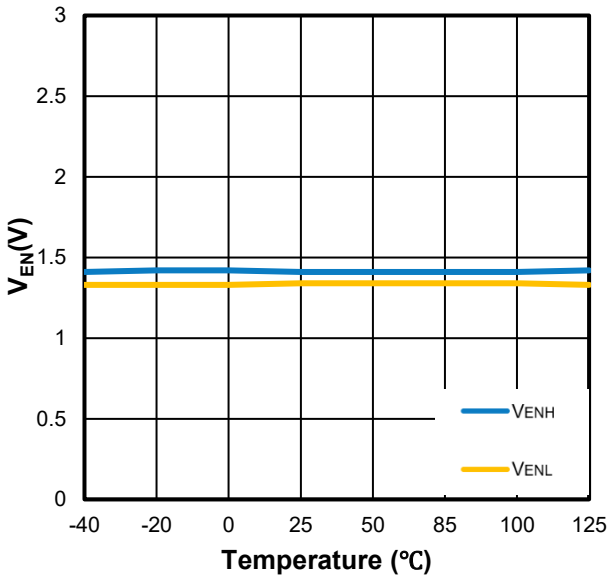


Figure 34. V_{EN} vs. Temperature

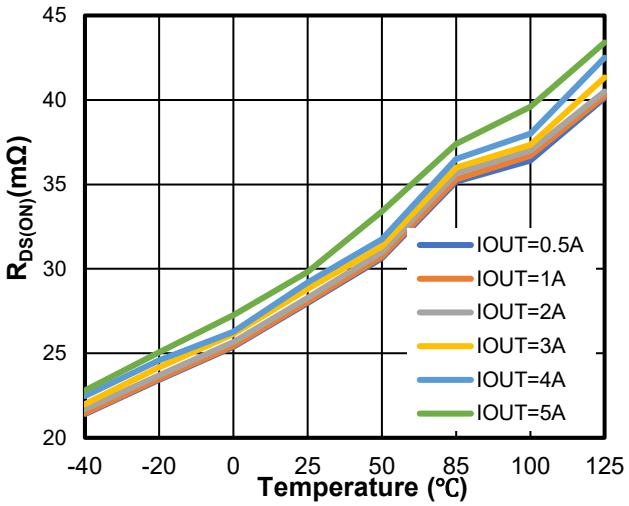


Figure 35. $R_{DS(ON)}$ vs. Temperature Across IOUT

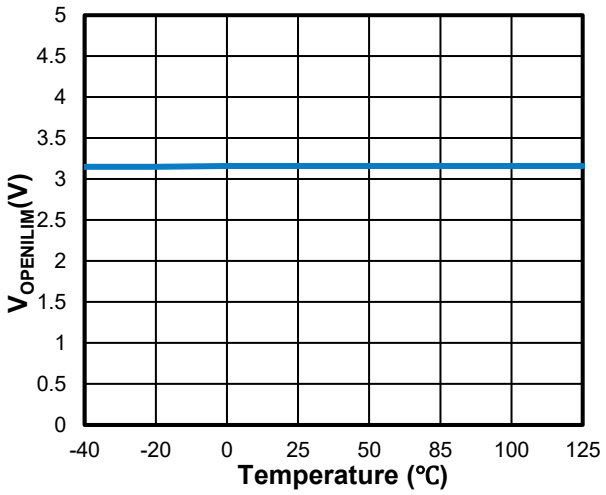


Figure 36. $V_{OPENILIM}$ vs. Temperature

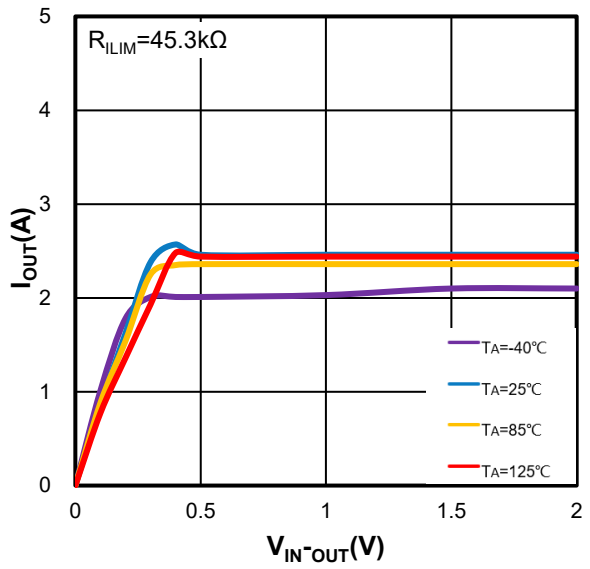


Figure 37. I_{OUT} vs. V_{IN-OUT}

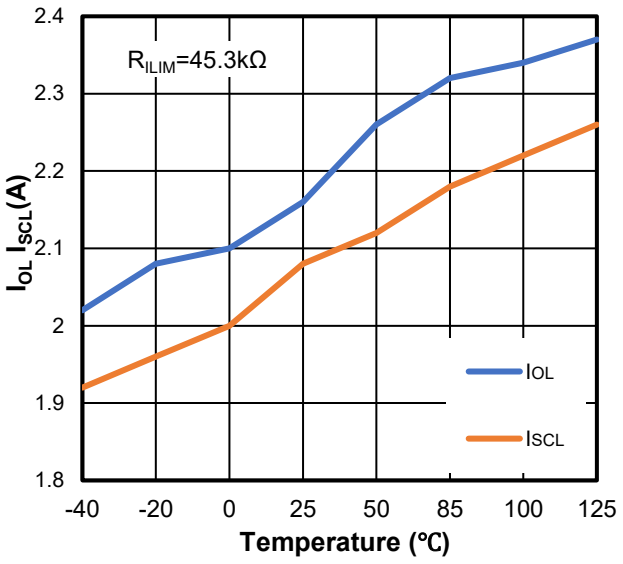


Figure 38. I_{OL} I_{SCL} vs. Temperature

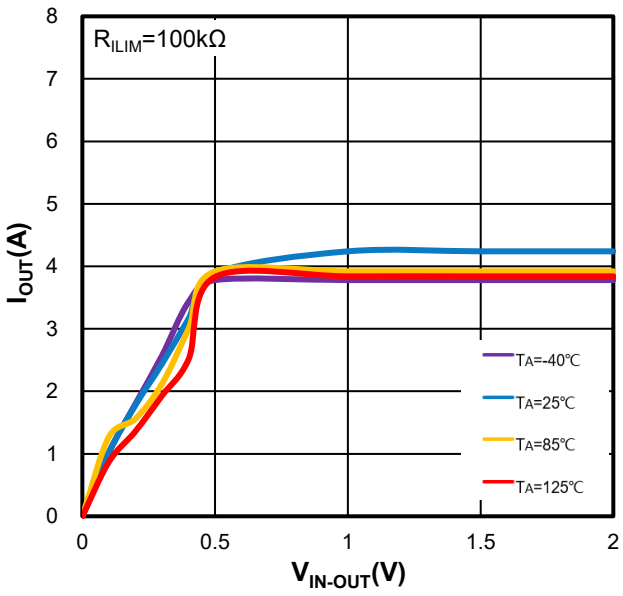


Figure 39. I_{OUT} vs. V_{IN-OUT}

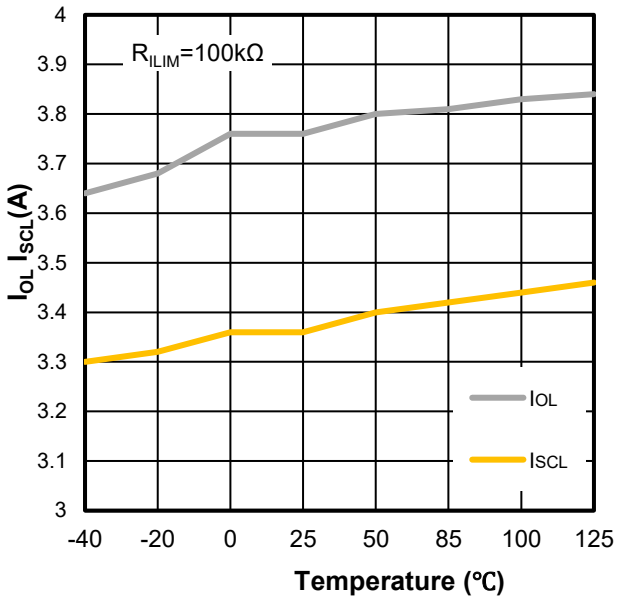


Figure 40. I_{OL} I_{SCL} vs. Temperature

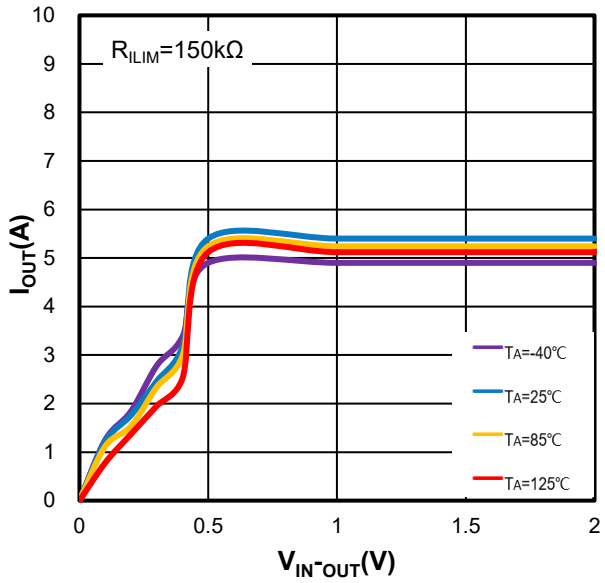


Figure 41. I_{OUT} vs. V_{IN-OUT}

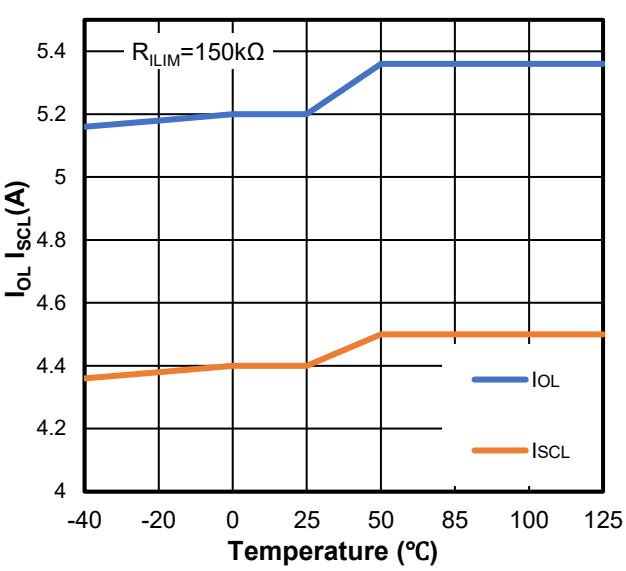


Figure 42. I_{OL} I_{SCL} vs. Temperature

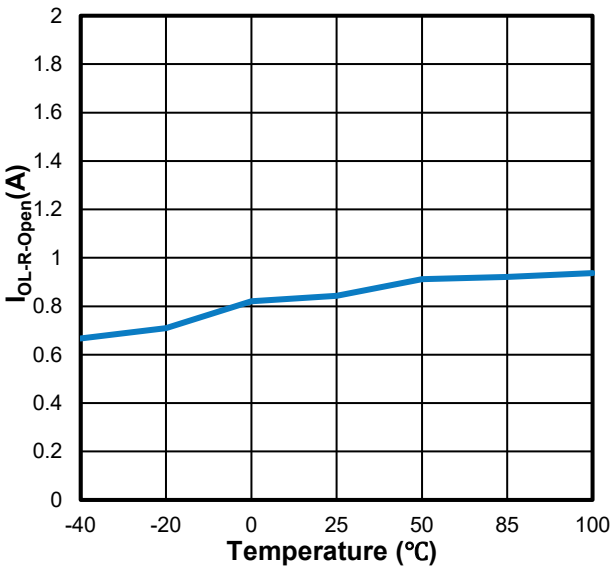


Figure 43. $I_{OL-R-Open}$ vs. Temperature

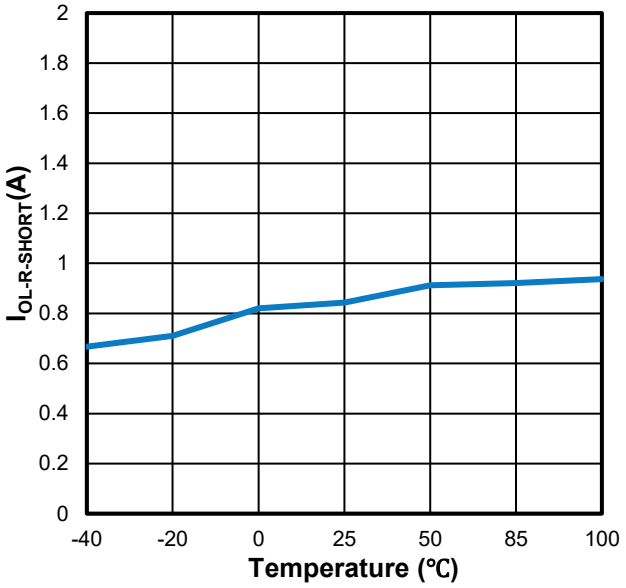


Figure 44. $I_{OL-R-SHORT}$ vs. Temperature

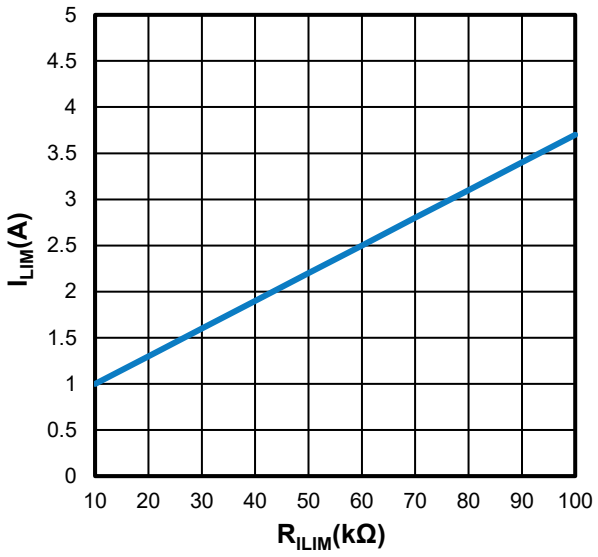


Figure 45. I_{LIM} vs. R_{ILIM}

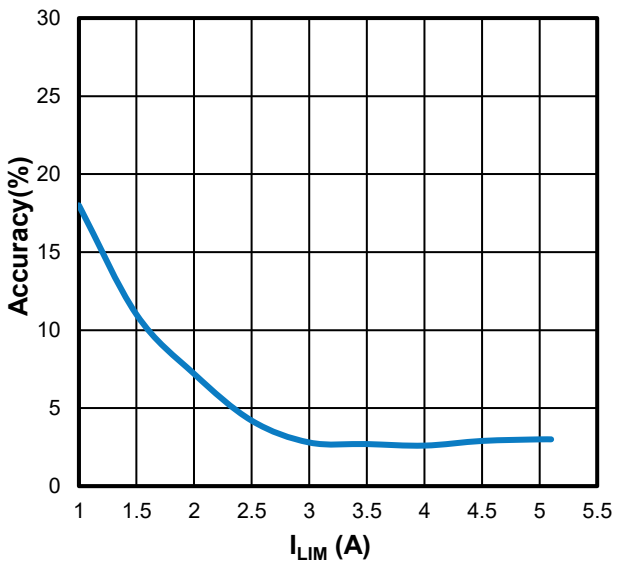


Figure 46. Accuracy vs. I_{LIM}

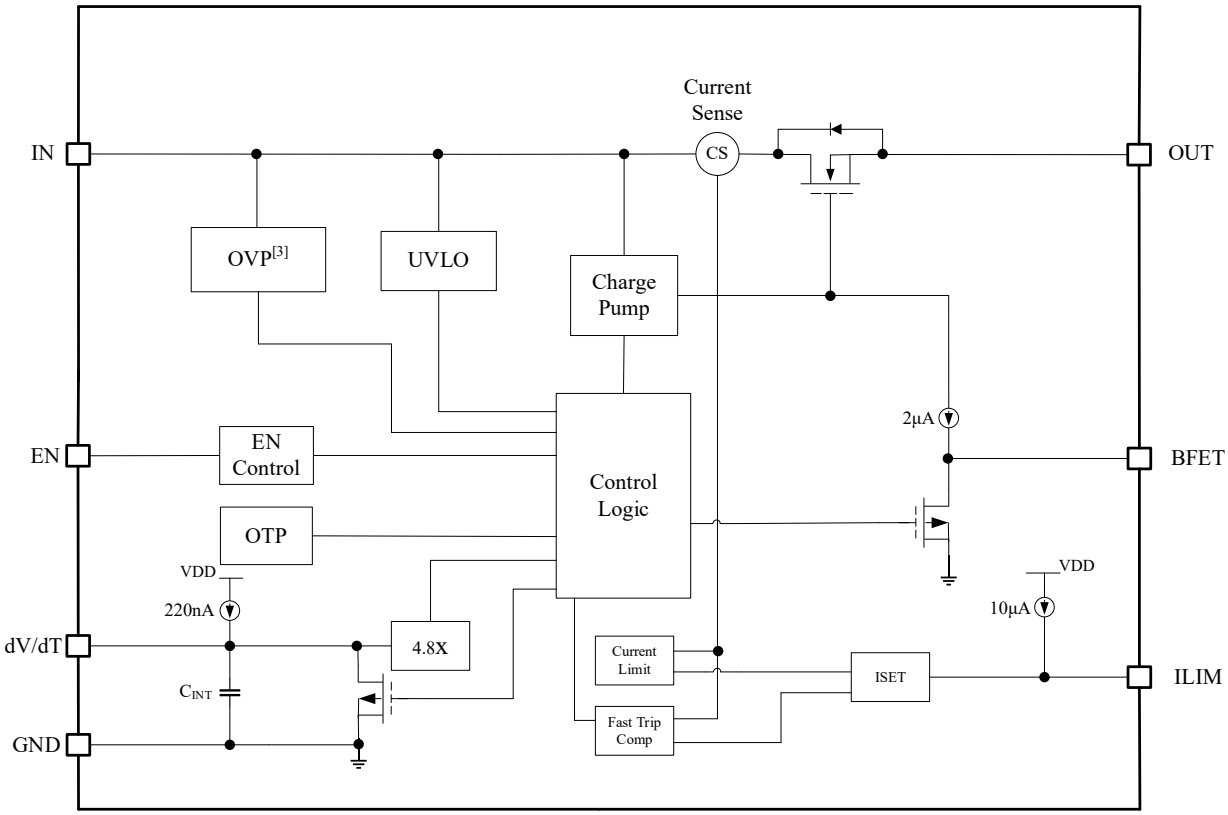
12. Function Description

12.1 Overview

The WP1507 is an e-fuse with an integrated power switch to manage the current, voltage and start-up voltage ramps of the connected load. The device starts operation by monitoring the IN bus. When IN exceeds the undervoltage lockout threshold and the EN/UVLO pin is held high, the internal MOSFET turns on and the chip begins operation, and when the EN/UVLO pin is held low, the internal MOSFET turns off. Current limit threshold is programmed with a resistor from ILIM to ground. The soft-start time is set with a capacitor from the dV/dT pin to the ground to limit the current surge during start-up. The device also integrates an over-temperature protection function, when the device temperature (T_J) exceeds T_{SHDN}, the thermal shutdown circuitry shuts down the internal MOSFET thereby disconnecting the load from the supply.

In WP1507-A/C/E, the output remains disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The WP1507-B/D/F device remains off during a cooling period until device temperature falls below T_{SHDN} – 20℃, after which it attempts to restart. This ON and OFF cycle continues until fault is cleared.

12.2 Block Diagram



Note 3: WP1507-A/B does not include this block

12.3 Feature Description

12.3.1 IN

A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V to 18 V for WP1507. The device can continuously sustain a voltage of 20 V on IN pin.

12.3.2 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum $t_{dV/dT}$) on the output. Equation governing slew rate at start-up is shown in Equation1:

$$\frac{dV_{OUT}}{dt} = \frac{I_{dV/dT} \times GAIN_{dV/dT}}{C_{dV/dT} + C_{INT}}$$

Where:

$I_{dV/dT}$ = 220nA (Typ.)
C_{INT} = 70pF (Typ.)
$GAIN_{dV/dT}$ = 4.85

$\frac{dV_{OUT}}{dt}$ = Desired output slew rate. (1)

The total ramp time ($t_{dV/dT}$) for 0 to VIN can be calculated using Equation2:

$$t_{dV/dT} = 10^6 \times V_{IN} \times (C_{dV/dT} + 70pF) \quad (2)$$

12.3.3 BFET

Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at IN. The BFET pin is controlled by either input UVLO event or EN/UVLO. BFET can source charging current to 2μA (Typ.) and sink (discharge) current from the gate of the external FET via a 26Ω internal discharge resistor to initiate fast turn off, typically < 1μs. Due to 2μA charging current, it is recommended to use > 10MΩ impedance when probing the BFET node.

$V_{EN/UVLO} > V_{EN_R}$	$V_{IN} > V_{UVLO_R}$	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

12.3.4 EN/UVLO

As an input pin, it controls both the ON and OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin turns off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor.

12.3.5 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After start-up event and during normal operation, current limit is set as shown in Equation3:

$$I_{OL} = 0.7 + 3 \times 10^{-5} \times R_{ILIM} \quad (3)$$

Choose closest standard value resistor with 1% tolerance.

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the WP1507 incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT} > I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over load current limit ($I_{FASTRIP} = 1.6 \times I_{OL}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to I_{OL}.

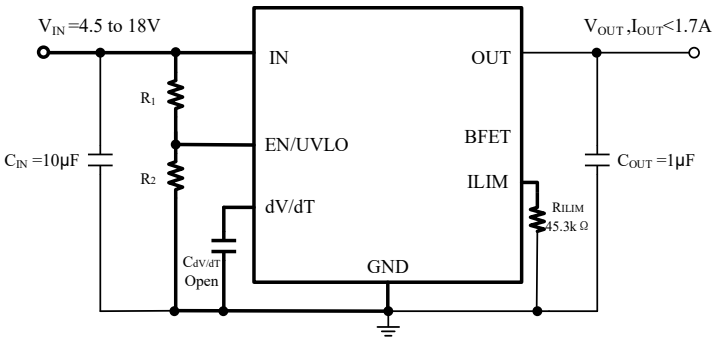
13. Application and Implementation

13.1 Application Information

The WP1507 is a smart e-Fuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

13.2 Typical Application

13.2.1 Simple 2.1-A e-Fuse Protection



Typical Application Schematic: Simple 2.1A e-Fuse

Note: R_1 and R_2 are optional, and only needed for external UVLO, not needed for internal UVLO which is controlled by EN. $R_1 \geq 1M\Omega$ is a must.

13.2.1.1 Design Requirements

The following table shows the design parameters for this application.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, V_{IN}	5V/12 V
Undervoltage lockout set point, $V_{(UV)}$	Default: V_{UVLO} = 4.3 V (R_1=1MΩ, R_2 open)
Load at start-up, $R_{L(SU)}$	8 Ω
Current limit, $I_{OL} = I_{ILIM}$	2.1A
Input capacitance, C_{IN}	10 μF
Load capacitance, C_{OUT}	1 μF
Maximum ambient temperature, T_A	85℃

13.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the WP1507.

13.2.1.2.1 Step by Step Design Procedure

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

13.2.1.2.2 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4:

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For $I_{OL} = I_{ILIM}$ = 2.1 A, from Equation 4, R_{ILIM} = 45.3kΩ, choose closest standard value resistor with 1% tolerance.

13.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R1 and R2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5:

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENH} \quad (5)$$

Where V_{ENH} = 1.4 V is enable voltage rising threshold.

Since R_1 and R_2 leak the current from input supply (V_{IN}), these resistors must be selected based on the

acceptable leakage current from input power supply (V_{IN}). The current drawn by R_1 and R_2 from the power supply {$I_{R12} = V_{IN} / (R_1 + R_2)$}.

However, leakage currents due to external active components connected to the resistor string can add error to

these calculations. So, the resistor string current, I_{R12} must be chosen to be 20x greater than the leakage current

expected.

For default UVLO of V_{UVR} = 4.3 V, select R_2 = OPEN, and R_1 = 1 MΩ. Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to V_{IN} = 12 V. It has to be connected through R_1 = 1 MΩ only, so that the pull-up current for EN/UVLO pin is limited to < 20 µA.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the

rising threshold, V_{UVLO}.This is calculated using Equation 6:

$$V_{(PFAIL)} = 0.96 \times V_{UVLO} \quad (6)$$

Where V_{UVLO} is 4.3 V, Power fail threshold set is: 4.1 V.

13.2.1.2.4 Setting Output Voltage Ramp Time ($t_{dV/dT}$)

For a successful design, the junction temperature of device must be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load. The ramp-up capacitor $C_{dV/dT}$ needed is calculated considering the two possible cases:

13.2.1.2.4.1 Case1: Start-Up without Load: Only Output Capacitance C_{OUT} Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using Equation8.

For WP1507, the inrush current is determined using Equation 7:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{dV/dT}} \quad (7)$$

Power dissipation during start-up is given by Equation 8:

$$P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (8)$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

13.2.1.2.4.2 Case2: Start-Up with Load: Output Capacitance C_{OUT} and Load Draws Current During Start-Up

When load draws current during the turn on sequence, there is additional power dissipated. Considering a resistive load during start-up ($R_{L(SU)}$), load current ramps up proportionally with increase in output voltage

during $t_{dV/dT}$ time. The average power dissipation in the internal FET during charging time due to resistive load is given by Equation9:

$$P_{D(Load)} = \frac{1}{6} \times \frac{V^2{}_{IN}}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during start-up is given by Equation 10:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

Total current during start-up is given by Equation 11:

$$I_{STARTUP} = I_{INRUSH} + I_L(t)$$
(11)

If $I_{STARTUP} > I_{OL}$, the device limits the current to I_{OL} and the current limited charging time is determined by Equation 12:

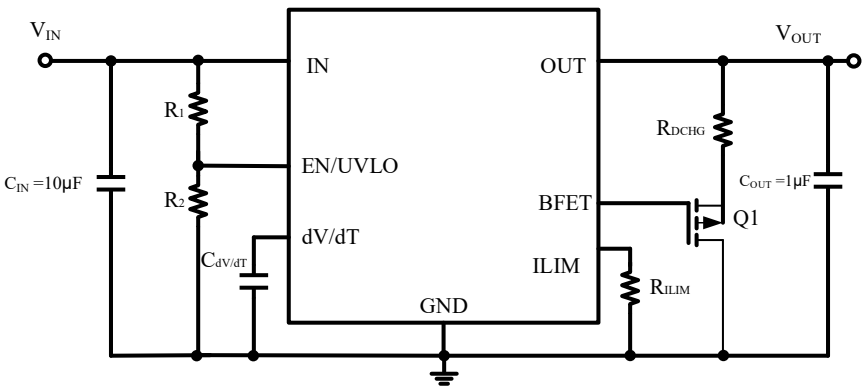
$$t_{dV/dT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{OL}}{I_{INRUSH}} - 1 + \ln \frac{I_{INRUSH}}{I_{OL} - \frac{V_{IN}}{R_{L(SU)}}} \right] \quad (12)$$

13.2.1.2.5 Support Component Selection—C_{IN}

C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. A value 10μF is recommended for C_{IN}.

13.2.2 Controlled Power Down using WP1507

When the device is disabled, the output voltage is left floating and power down profile is entirely dictated by the load. In some applications, this can lead to undesired activity as the load is not powered down to a defined state. Controlled output discharge can ensure the load is turned off completely and not in an undefined operational state. The BFET pin in WP1507 facilitates Quick Output Discharge (QOD) function as illustrated in the following figure. When the device is/gets disabled, the BFET pin pulls low which enables the external P MOSFET Q1 for discharge feature to function. The output voltage discharge rate is dictated by the output capacitor C_{OUT}, the discharge resistance R_{DCHG} and the load.



Circuit Implementation with Quick Output Discharge Function

14. Power Supply Recommendations

The device is designed for supply voltage range of 4.5 V ≤ VIN ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 10 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

14.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the Absolute Maximum Ratings of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A ceramic capacitor (C_{IN} = 10 µF) to absorb the energy and dampen the transients.

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the Absolute Maximum Ratings of the device.

14.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate the device performance. We have evaluation modules for different packages, you can contact us at the end to get the evaluation module or schematic.

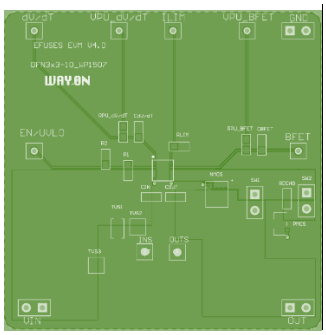
The module names are listed in the following table.

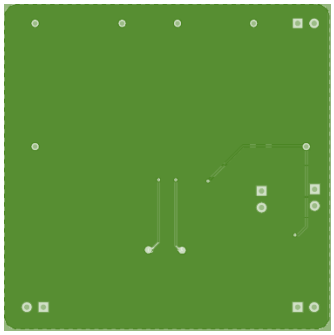
NAME	PACKAGE	EVALUATION MODULE
WP1507	DFN-3×3-10L	EFUSE EVM V4.0 DFN3X3-10_WP1507

Layout Guidelines

For best performance, all traces should be as short as possible, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for IN, OUT, and GND will help minimize parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Layout Example





16. Naming Conventions

WP AB CC-D EEE F

WP: WAYON Protection IC;

A: Product Category –1: E-fuse;

B: Maximum Output Current – 5: ≤5A;

CC: Serial number;

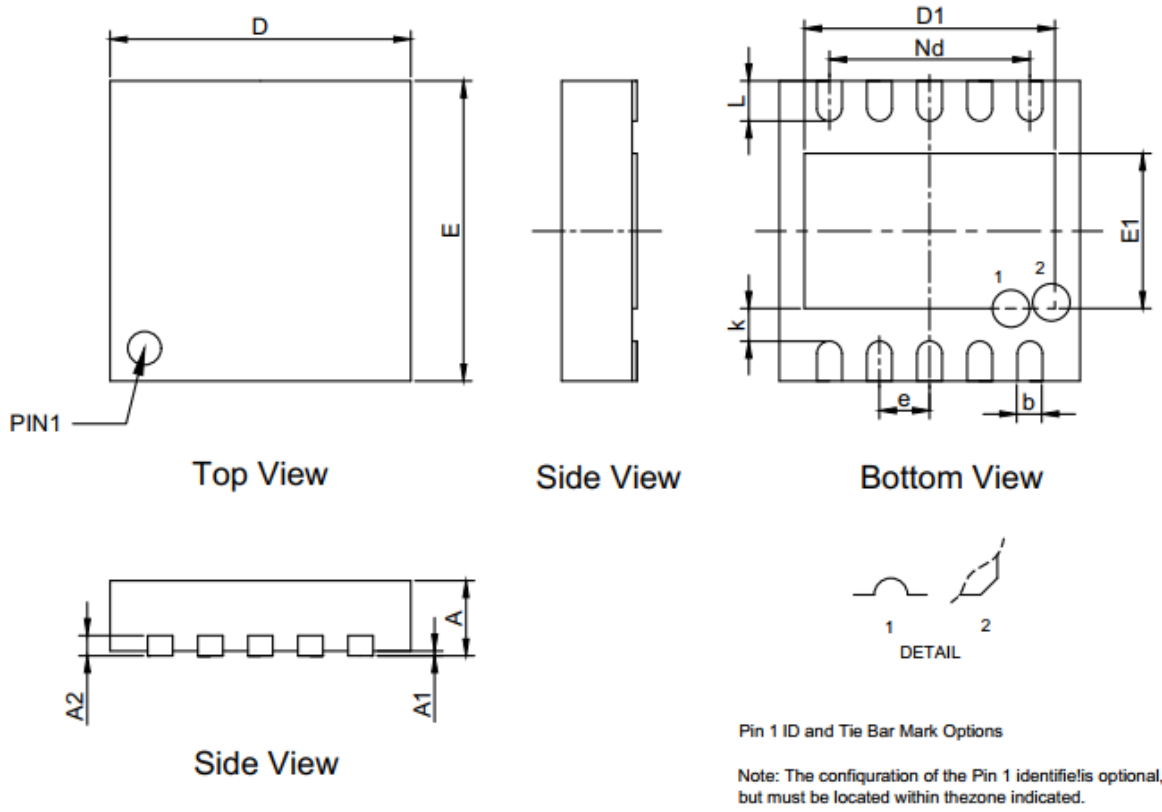
D: Version;

EEE: Package – FEA: DFN-3×3-10L;

F: R-Reel & T-tube;

17. Package Information

DFN 3*3-10L



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2		0.203REF	
b	0.15	0.25	0.35
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.20	-	2.60
E1	1.45	-	1.90
e		0.50BSC	
Nd		2.00BCS	
k	0.20	-	-
L	0.30	0.40	0.50

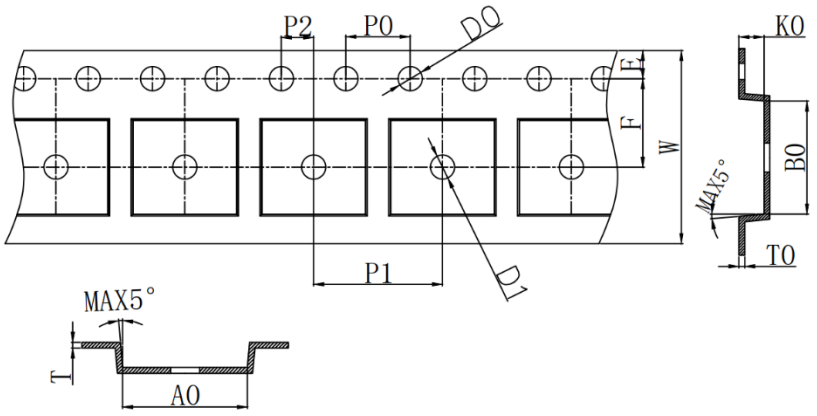
18. Ordering Information

PART NUMBER	OVP CLAMP	FAULT RESPONSE	PACKAGE	PACKING QUANTITY	MARKING*
WP1507-AFEAR	-	Latched	DFN-3×3-10L	3k/Reel	WP1507 A XXXX
WP1507-BFEAR	-	Auto Retry	DFN-3×3-10L	3k/Reel	WP1507 B XXXX
WP1507-CFEAR	6.1V	Latched	DFN-3×3-10L	3k/Reel	WP1507 C XXXX
WP1507-DFEAR	6.1V	Auto Retry	DFN-3×3-10L	3k/Reel	WP1507 D XXXX
WP1507-EFEAR	15V	Latched	DFN-3×3-10L	3k/Reel	WP1507 E XXXX
WP1507-FFEAR	15V	Auto Retry	DFN-3×3-10L	3k/Reel	WP1507 F XXXX

* XXXX is variable.

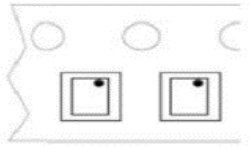
19. Package specification

19.1 Carrier belt

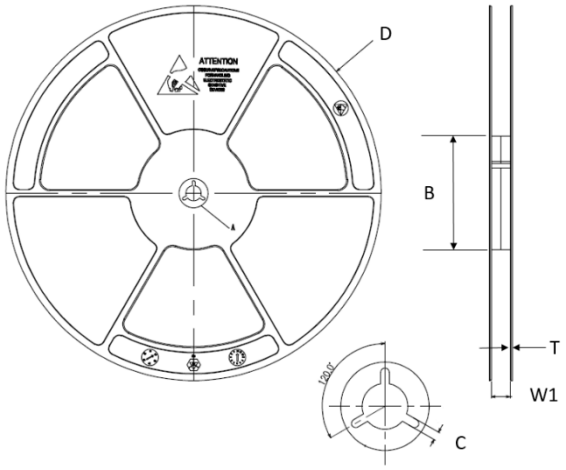


A0(mm)	B0(mm)	K0(mm)	D0(mm)	D1(mm)	P0(mm)
3.20~3.45	3.25~3.45	0.90~1.23	1.50~1.60	1.50~1.75	3.90~4.10
P1(mm)	**P2(mm)**	**W(mm)**	**T(mm)**	**E(mm)**	**F(mm)**
7.90~8.10	1.95~2.05	11.90~12.30	0.23~0.35	1.65~1.85	5.45~5.55

19.2 Placement direction

PIN1	

19.3 Reels: 13inch



D(mm)	W1(mm)	T(mm)	B(mm)	C(mm)
329~331	12.4~13.0	1.8~3.1	99.5~100.5	1.5~2.5

Contact Information

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Specifications are subject to change without notice.
The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

Product Specification Statement

- The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.
- The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. WAYON shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and WAYON assumes no responsibility for the application of the product.
- WAYON strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, WAYON cannot guarantee that the information provided in the product specification is entirely accurate and error-free. WAYON shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications. WAYON reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with WAYON to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult WAYON in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.
- Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.
- The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. WAYON shall assume no responsibility for any consequences resulting from such usage.
- Users should also comply with relevant laws, regulations, policies, and standards when using the product specification. Users are responsible for the risks and liabilities arising from the use of the product specification and must ensure that it is not used for illegal purposes. Additionally, users should respect the intellectual property rights related to the product specification and refrain from infringing upon any third-party legal rights. WAYON shall assume no responsibility for any disputes or controversies arising from the above-mentioned issues in any form.