WP5602

USB Type-C Port Protector: Short-to-VBUS Overvoltage and IEC ESD Protection

1. General Description

The WP5602 is a USB Type-C port protection chip that provides 20-V Short-to-VBUS overvoltage and IEC ESD protection.

By integrating low on-resistance power switch and low capacitance TVS, the WP5602 protects USB Type-C ports CC，SBU and D+/D- that undergoing overvoltage and IEC 61000-4-2 system level ESD without interfering with normal operation.

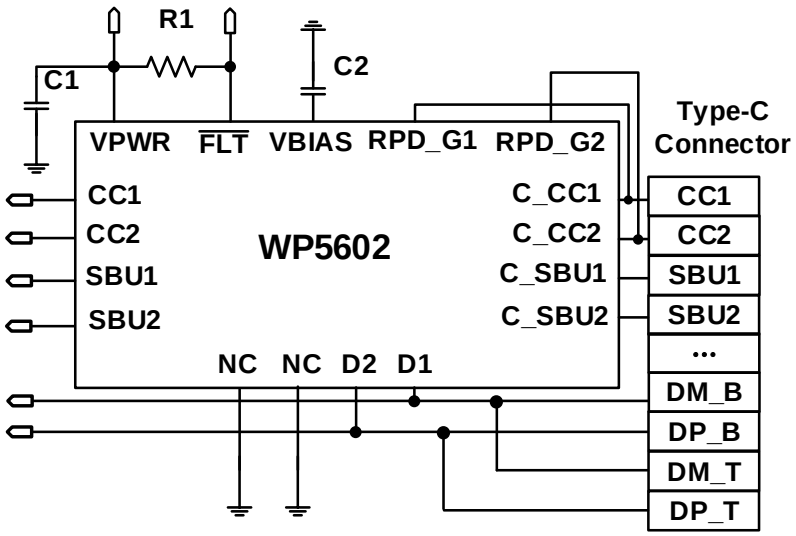
2. Features

- Short to VBUS Overvoltage Protection for CC1, CC2, SBU1 and SBU2
- IEC 61000-4-2 ESD Protection for CC1, CC2, SBU1, SBU2, DP, DM
- Low on-resistance protection FET for CC1 and CC2 passing 600 mA V_{CONN} current
- Fast OVP response for CCX and SBUX
- CC Dead Battery Resistors integrated for handling dead battery use case in mobile devices
- Package: 3-mm × 3-mm QFN

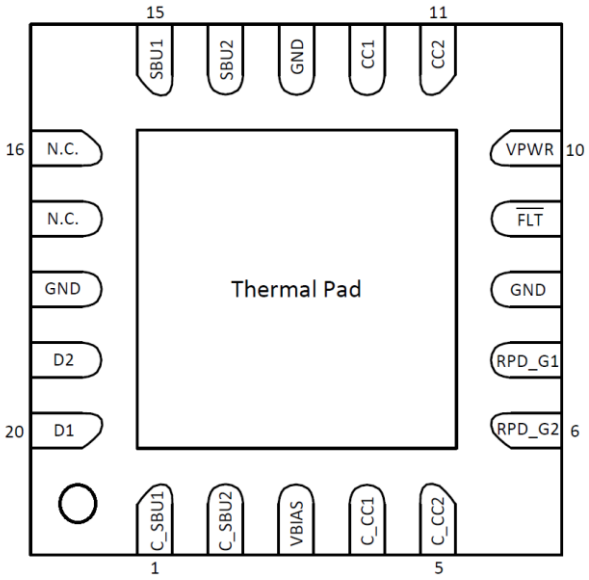
3. Applications

- Laptop PC
- Tablets
- Smart phones
- Monitors and TVS
- Docking Stations

4. Typical Application



5. Pin Configuration



6. Pin Description

PIN NUMBER	PIN NAME	I/O	PIN FUNCTIONS
1	C_SBU1	I/O	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector.
2	C_SBU2	I/O	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector.
3	VBIAS	Power	Pin for ESD support capacitor. Place a 0.1-μF capacitor on this pin to ground.
4	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector.
5	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector.
6	RPD_G2	I/O	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
7	RPD_G1	I/O	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
8	GND	GND	Ground.
9	$\overline{\text{FLT}}$	O	Open drain for fault reporting. Under over temperature & over voltage conditions, pull low. Otherwise stay high-Z. Connect to VPWR by external resistor.
10	VPWR	Power	2.7V – 5.5V power supply.

PIN NUMBER	PIN NAME	I/O	PIN FUNCTIONS
11	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller.
12	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller.
13	GND	GND	Ground.
14	SBU2	I/O	System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX.
15	SBU1	I/O	System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX.
16	NC	I/O	Unused pin. Connect to Ground.
17	NC	I/O	Unused pin. Connect to Ground.
18	GND	GND	Ground.
19	D2	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector.
20	D1	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector.
-	Thermal Pad	GND	Internally connected to GND. Used as a heatsink. Connect to the PCB GND plane.

7. Absolute Maximum Ratings [1]

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		RATING	UNIT
V_I	Input Voltage	VPWR	-0.3 to 6	V
		RPD_G1, RPD_G2	-0.3 to 24	V
V_O	Output Voltage	$\overline{FLT}$	-0.3 to 6	V
		VBIAS	-0.3 to 24	V
V_{IO}	I/O Voltage	D1, D2	-0.3 to 6	V
		CC1, CC2, SBU1, SBU2	-0.3 to 6	V
		C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3 to 24	V
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]		40	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance [2]		23	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance [2]		10	℃/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance [2]		4.5	℃/W
$T_{J(MAX)}$	Maximum Junction Temperature		150	℃
T_A	Operating Free Air Temperature		-40 to 85	℃
T_{STG}	Storage Temperature		-65 to 150	℃

NOTE 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The above measurement conditions are based on JEDEC STD.51.

8. ESD Ratings—JEDEC Specification

PARAMETER		VALUE	UNIT
Electrostatic Discharge	Human-Body Model (HBM), Per ANSI/ESDA/JEDEC JS-001[3]	±6000	V
	Charged-Device Model (CDM), Per ANSI/ESDA/JEDEC JS-002[4]	±2000	V
	Latch-up model, per JEDEC JESD78F-2022	±800	mA

NOTE 3: JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±6000 V may actually have higher performance.

NOTE 4: JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

9. ESD Ratings—IEC Specification

PARAMETER			VALUE	UNIT
Electrostatic Discharge	IEC 61000-4-2, D1, D2	Contact Discharge	±15000	V
		Air-gap Discharge	±30000	
	IEC 61000-4-2, C_CC1, C_CC2	Contact Discharge	±10000	
		Air-gap Discharge	±20000	
	IEC 61000-4-2, C_SBU1, C_SBU2	Contact Discharge	±10000	
		Air-gap Discharge	±20000	
Lightning and Surge	IEC 61000-4-5, C_CC1, C_CC2, C_SBU1, C_SBU2		±35	V

10. Recommended Operating Conditions

(T_A=25℃, unless otherwise noted)

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{IN}	Input Voltage	VPWR	2.7	3.3	5.5	V
		RPD_G1, RPD_G2	0		5.5	V
V_{OUT}	$\overline{FLT}$ Pull-up Resistor Power Rail		2.7		5.5	V
V_{IO}	I/O Voltage	D1, D2	-0.3		5.5	V
		CC1, CC2, C_CC1, C_CC2	0		5.5	V
		SBU1, SBU2, C_SBU1, C_SBU2	0		4.3	V
I_{VCONN}	V_{CONN} Current	Current flowing into CC1/2 and flowing out of C_CC1/2, $V_{CCX} – V_{C_CCX} \leq 250$ mV			600	mA
I_{VCONN}	V_{CONN} Current	Current flowing into CC1/2 and flowing out of C_CC1/2, $T_J \leq 105$℃			600	mA
I_{VCONN}	V_{CONN} Current	Current flowing into CC1/2 and flowing out of C_CC1/2, $T_J \leq 85$℃			1.25	A
	External Components [5]	$\overline{FLT}$ Pull-up Resistance	1.7		300	kΩ
		VBIAS Capacitance [6]		0.1		μF
		VPWR Capacitance	0.3	1		μF

NOTE 5: For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented must be within the minimum and maximums listed in the table.

NOTE 6: The VBIAS pin requires a minimum 35-V_{DC} rated capacitor. A 50-V_{DC} rated capacitor is recommended to reduce capacitance derating.

11. Electrical Characteristics

(T_A=25℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
CC OVP Switches						
R_{ON}	On resistance of CC OVP FETs, $T_J \le 85$ ℃	CCX = 5.5 V		300	600	mΩ
R_{ONFLAT}	On resistance flatness	Sweep CCX voltage between 0V and1.2V			5	mΩ
C_{ON_CC}	Equivalent on capacitance	Capacitance from C_CCX or CCX to GND. V_{C_CCX}/V_{CCX} = 0 V to 1.2 V, f = 400 kHz	30	74	90	pF
R_{D_DB}	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of RD and FET in series	V_{C_CCX} = 2.6 V	4.1	5.1	6.1	kΩ
V_{TH_DB}	Threshold voltage of the pulldown FET in series with RD during dead battery	I_{CC} = 80 μA	0.5	0.9	1.2	V
V_{OVPCC}	OVP threshold on CC pins	Place 5.5 V on C_CCX. Step up C_CCX until the $\overline{FLT}$ pin is asserted	5.75	6	6.2	V
V_{OVPCC_HYS}	Hysteresis on CC OVP	Place 6.5 V on C_CCX. Step down the voltage on C_CCX until the $\overline{FLT}$ pin is deasserted. Measure difference between rising and falling OVP threshold for CC		50		mV
BW_{ON}	On bandwidth single ended (–3 dB)	Measure the –3-dB bandwidth from C_CCX to CCX. Single ended measurement, 50Ω system V_{CM} = 0.1 V to 1.2 V		100		MHz
V_{STBUS_CC}	Short-to-VBUS tolerance on the CC pins	Hot-Plug C_CCX with a 1meter USB Type C Cable, place a 30-Ω load on CCX			24	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{STBUS_CC_CLAMP}$	Short-to-VBUS system-side clamping voltage on the CC pins (CCX)	Hot-Plug C_CCX with a 1-meter USB Type C Cable. Hot-Plug voltage C_CCX = 24 V. VPWR = 3.3 V. Place a 30Ω load on CCX		8		V
SBU OVP Switches						
R_{ON}	On resistance of SBU OVP FETs	SBUX = 3.6 V, –40℃ ≤ T_J ≤ +85℃		3.5	6.5	Ω
R_{ONFLAT}	On resistance flatness	Sweep SBUX voltage between 0 V and 3.6 V. –40℃ ≤ T_J ≤ +85℃		1	1.5	Ω
C_{ON_SBU}	Equivalent on capacitance	Capacitance from SBUX or C_SBUX to GND. Measure at V_{C_SBUX}/V_{SBUX} = 0.3 V to 3.6 V		9		pF
V_{OVPSBU}	OVP threshold on SBU pins	Place 3.6 V on C_SBUX. Step up C_SBUX until the $\overline{FLT}$ pin is asserted	4.3	4.5	4.75	V
V_{OVPSBU_HYS}	Hysteresis on SBU OVP	Place 5 V on C_CCX. Step down the voltage on C_CCX until the $\overline{FLT}$ pin is deasserted. Measure difference between rising and falling OVP threshold for C_SBUX		60		mV
BW_{ON}	On bandwidth single ended (–3 dB)	Measure the –3-dB bandwidth from C_SBUX to SBUX. Single ended measurement, 50-Ω system. V_{CM} = 0.1 V to 3.6 V		1000		MHz
X_{TALK}	Crosstalk	Measure crosstalk at f = 1 MHz from SBU1 to C_SBU2 or SBU2 to C_SBU1. V_{CM1} = 3.6 V, V_{CM2}=0.3V. Be sure to terminate open sides to 50 Ω		-80		dB
V_{STBUS_SBU}	Short-to-VBUS tolerance on the SBU pins	Hot-Plug C_SBUX with a 1-meter USB Type C Cable. Put a 40Ω resistor to GND on SBUX			24	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{STBUS_SBU_CLAMP}$	Short-to-VBUS system-side clamping voltage on the SBU pins (SBUX)	Hot-Plug C_SBUX with a 1-meter USB Type C Cable. Hot-Plug voltage V_{C_SBUX} = 24 V. V_{PWR} = 3.3 V. Put a 40Ω resistor to GND on SBUX		8		V
Power Supply and Leakage Currents						
V_{PWR_UVLO}	VPWR under voltage lockout	Place 1 V on VPWR and raise voltage until SBU or CC FETs turn on	2.1	2.3	2.5	V
$V_{PWR_UVLO_HYS}$	VPWR UVLO hysteresis	Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis		10		mV
I_{VPWR}	VPWR supply current	V_{PWR} = 3.3 V (Typical), –40℃ ≤ T_J ≤ 85℃		70	120	μA
I_{CC_LEAK}	Leakage current for CC pins when device is powered	V_{PWR} = 3.3 V, V_{C_CCX} = 3.6 V, CCX pins are floating, measure leakage into C_CCX pins. Result must be same if CCX side is biased and C_CCX is left floating.			5	μA
I_{SBU_LEAK}	Leakage current for SBU pins when device is powered	V_{PWR} = 3.3 V, V_{C_SBUX} = 3.6V, SBUX pins are floating, measure leakage into C_SBUX pins. Result must be same if SBUX side is biased and C_SBUX is left floating. –40℃ ≤ T_J ≤ 85℃			3.5	μA
$I_{C_CC_LEAK_OVP}$	Leakage current for CC pins when device is in OVP	V_{PWR} = 0 V or 3.3 V, V_{C_CCX} = 24V, CCX pins are set to 0 V, Measure leakage into C_CCX pins			200	μA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
$I_{C_SBU_LEAK_OVP}$	Leakage current for SBU pins when device is in OVP	V_{PWR} = 0 V or 3.3 V, V_{C_SBUX} = 24 V, SBUX pins are set to 0 V, measure leakage into C_SBUX pins			200	µA
$I_{CC_LEAK_OVP}$	Leakage current for CC pins when device is in OVP	V_{PWR} = 0 V or 3.3 V, V_{C_CCX} = 24 V, CCX pins are set to 0 V, measure leakage out of CCX pins			30	µA
$I_{SBU_LEAK_OVP}$	Leakage current for SBU pins when device is in OVP	V_{PWR} = 0 V or 3.3 V, V_{C_SBUX} = 24 V, SBUX pins are set to 0 V, measure leakage out of SBUX pins	–1		1	µA
I_{DX_LEAK}	Leakage current for Dx pins	V_{DX} = 3.6 V, measure leakage into Dx pins			1	µA
$\overline{FLT}$ Pin						
V_{OL}	Low-level output voltage	I_{OL} = 3 mA. Measure the voltage at the $\overline{FLT}$ pin			0.4	V
Over Temperature Protection						
T_{SD_RISING}	The rising over-temperature protection shutdown threshold			170		℃
$T_{SD_FALLING}$	The falling over-temperature protection shutdown threshold			135		℃
T_{SD_HYST}	The over-temperature protection shutdown threshold hysteresis			35		℃
Dx ESD Protection						
V_{RWM_POS}	Reverse stand-off voltage from Dx to GND	Dx to GND. IDX ≤1 µA			5.5	V
V_{RWM_NEG}	Reverse stand-off voltage from GND to Dx	GND to Dx			0	V
V_{BR_POS}	Break-down voltage from Dx to GND	Dx to GND. IBR = 1 mA	7			V
V_{BR_NEG}	Break-down voltage from GND to Dx	GND to Dx. IBR = 8 mA	0.6			V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
C_{IO}	Capacitance Dx to GND or GND to Dx	f = 1 MHz, VIO = 2.5 V		2.5		pF
ΔC_{IO}	Differential capacitance between two Dx pins	f = 1 MHz, VIO = 2.5 V		1		pF
R_{DYN}	Dynamic on-resistance Dx IEC clamps	Dx to GND or GND to Dx		0.4		Ω
Power-On and Off Timings						
t_{ON}	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on			0.15		ms
t_{ON_DB}	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are turned off			5.7		ms
dV_{PWR_OFF}/d_t	Minimum slew rate allowed to guarantee CC and SBU FETs turnoff during a power off		–0.5			V/µs
Over Voltage Protection						
$t_{OVP_RESPONSE_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turnoff			80		ns
$t_{OVP_RESPONSE_SBU}$	OVP response time on the SBU pins. Time from OVP asserted until OVP FETs turnoff			130		ns
$t_{OVP_RECOVERY_CC_1}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on			0.6		ms
$t_{OVP_RECOVERY_CC_1_DB}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. OVP must be removed for CC FETs to turn back on			5		ms
$t_{OVP_RECOVERY_SBU_1}$	OVP recovery time on the SBU pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on			0.5		ms
$t_{OVP_RECOVERY_CC_2}$	OVP recovery time on the CC pins. Time from OVP Removal until CC FETs turn back on, if device has been in OVP > 0.6 ms			0.2		ms
$t_{OVP_RECOVERY_CC_2_DB}$	OVP recovery time on the CC pins. Time from OVP Removal until CC FETs turn back on and dead battery resistors turn off, if device has been in OVP > 0.6 ms			5		ms

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
$t_{OVP_RECOVERY_SBU_2}$	OVP recovery time on the SBU pins. Time from OVP Removal until SBU FETs turn back on, if device has been in OVP > 0.6 ms		0.1		ms
$t_{OVP_FLT_ASSETION}$	Time from OVP asserted to $\overline{FLT}$ assertion		20		μs
$t_{OVP_FLT_DEASSERTION}$	Time from CC FET turn on after an OVP to $\overline{FLT}$ Deassertion		5		ms

12. Typical Performance Characteristics

(V_{PWR} = 3.3V, T_A = 25℃, C_1 = 1μF, C_2 = 0.1μF, R_1 = 100kΩ, unless otherwise noted)

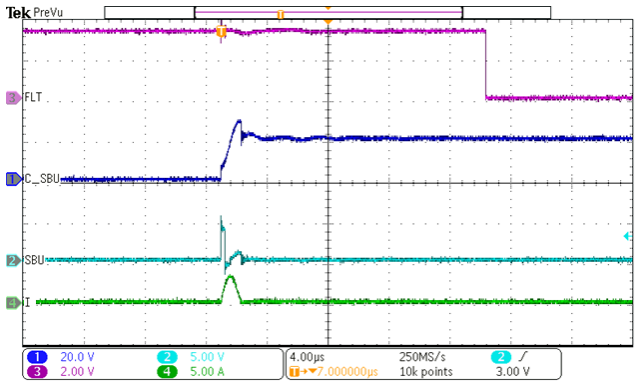


Fig. 1 SBU Short to VBUS 20 V

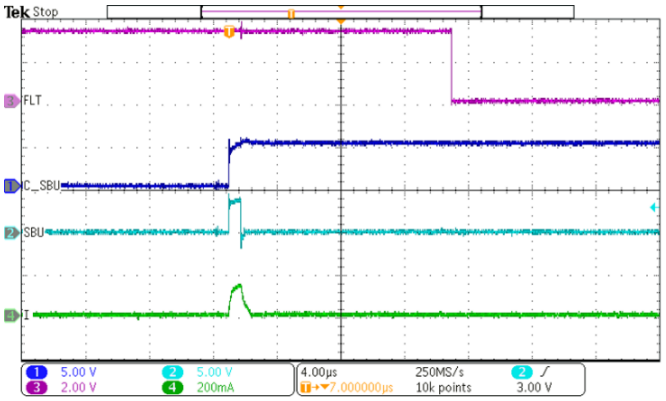


Fig. 2 SBU Short to VBUS 5 V

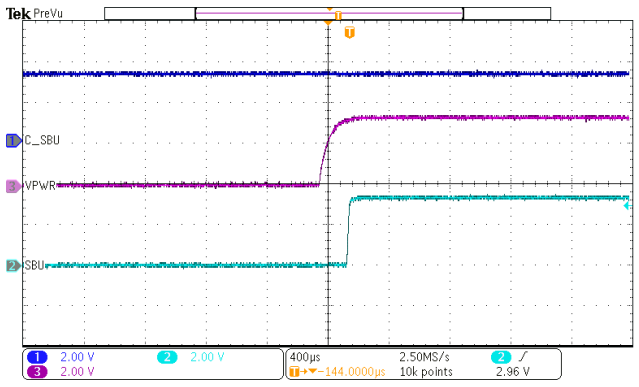


Fig. 3 SBU FET Turn-on Timing

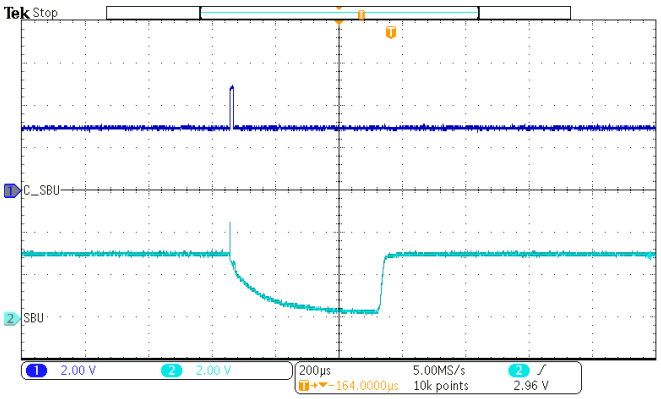


Fig. 4 SBU OVP removed to turn on recovery time

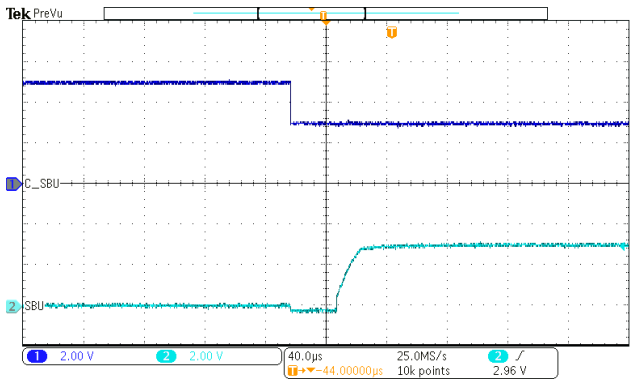


Fig. 5 SBU OVP removed to turn on recovery time
（OVP > 0.6ms）

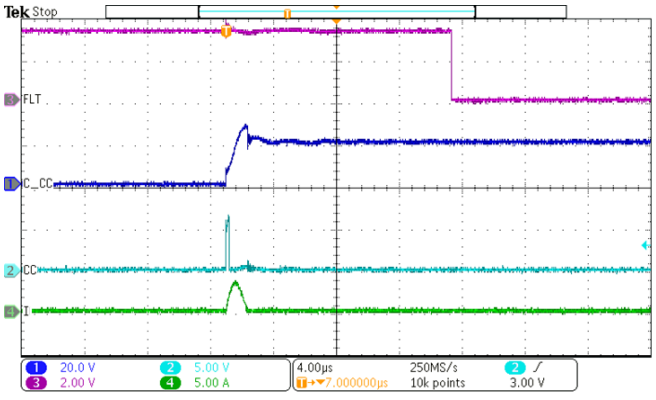


Fig. 6 CC Short to VBUS 20 V

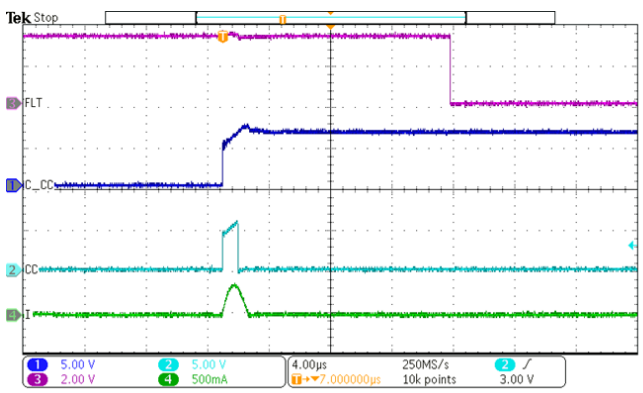


Fig. 7 CC Short to VBUS 6.5 V

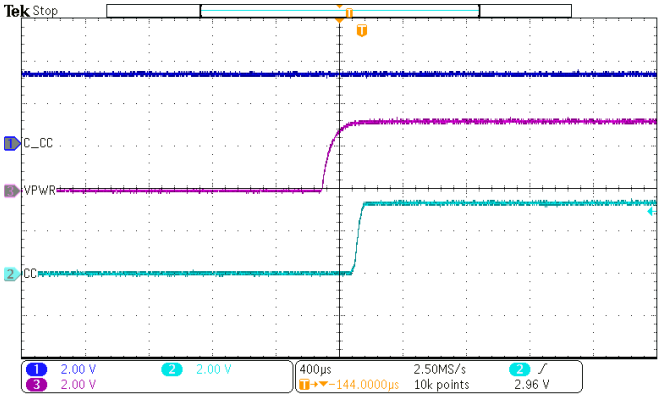


Fig. 8 CC FET Turn-on Timing

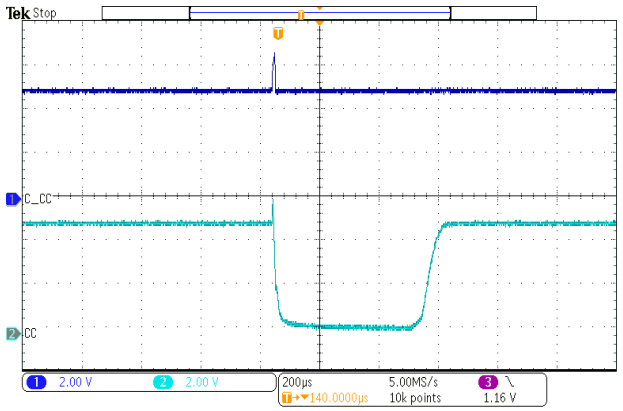


Fig. 9 CC OVP removed to turn on recovery time

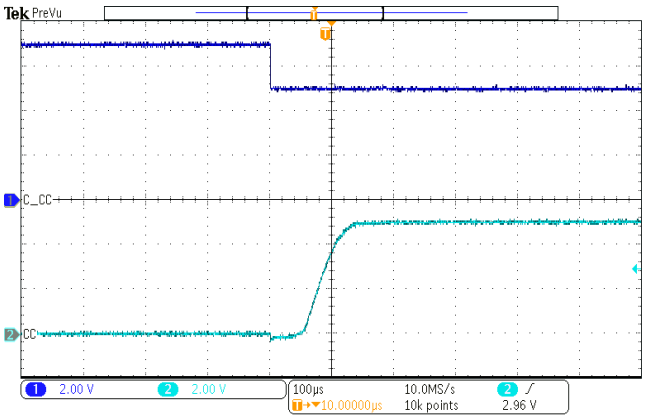


Fig. 10 CC OVP removed to turn on recovery time

（OVP > 0.6 ms）

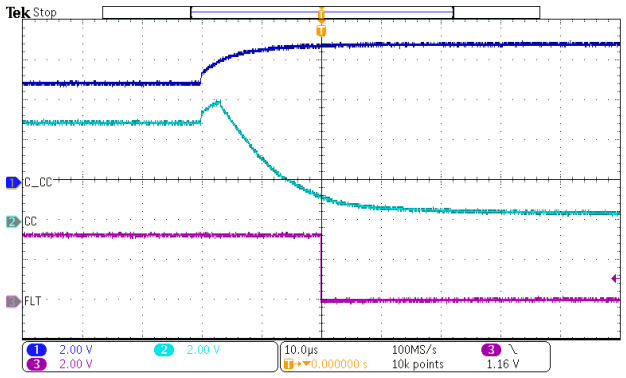


Fig. 11 Time from OVP asserted to FLT assertion

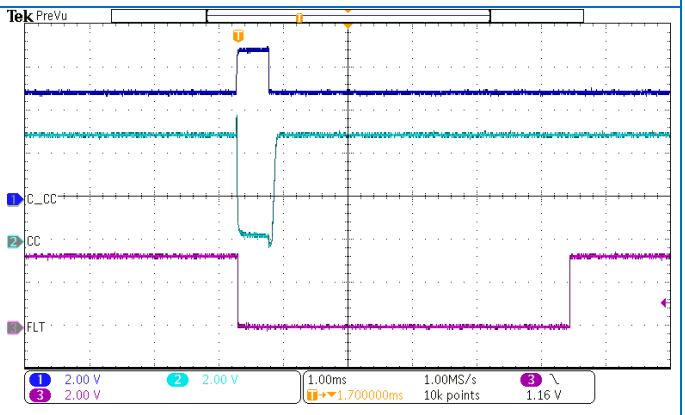


Fig. 12 Time from CC FET turn on after an OVP to $\overline{FLT}$ deassertion

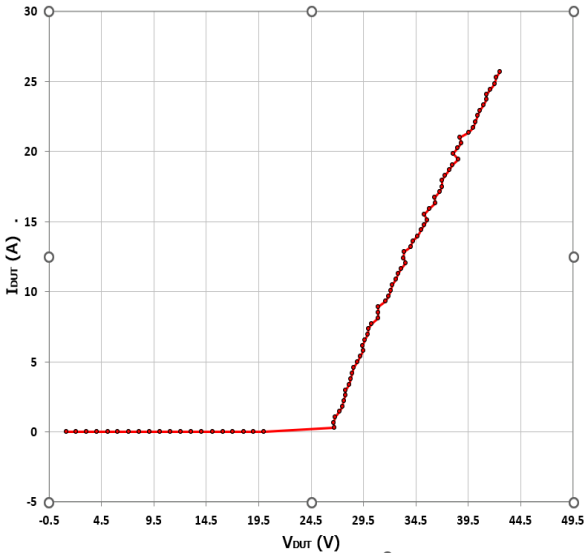


Fig. 13 C_SBU TLP Curve Unpowered

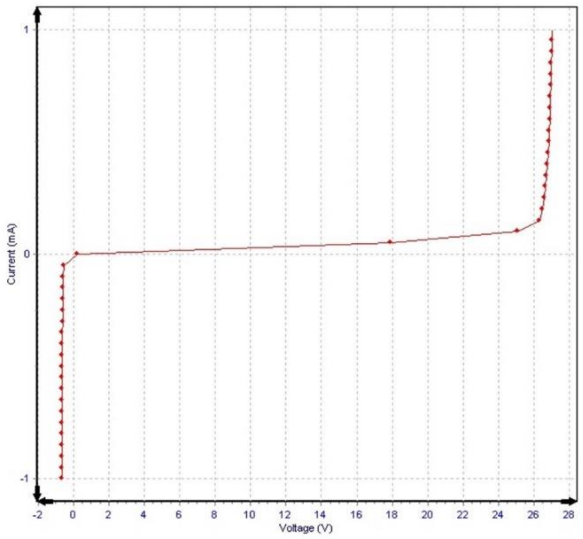


Fig. 14 SBU IV Curve

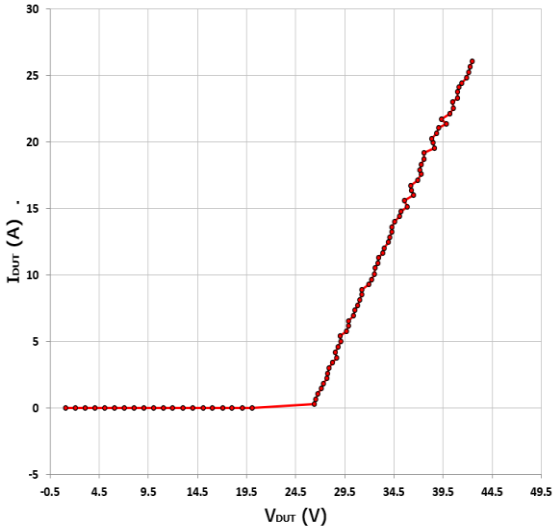


Fig. 15 C_CC TLP Curve Unpowered

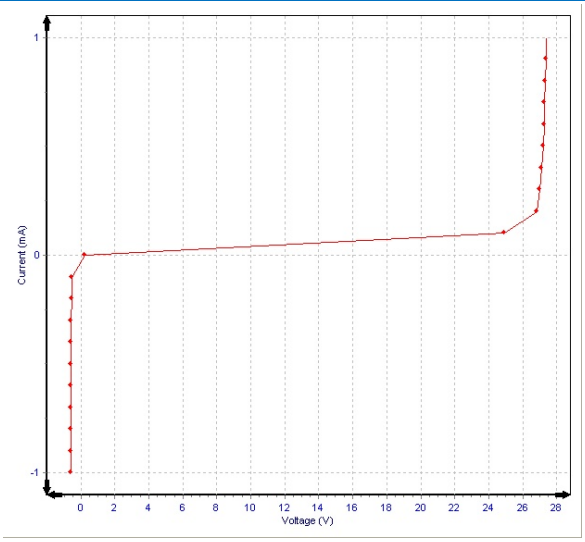


Fig. 16 C_CC IV Curve

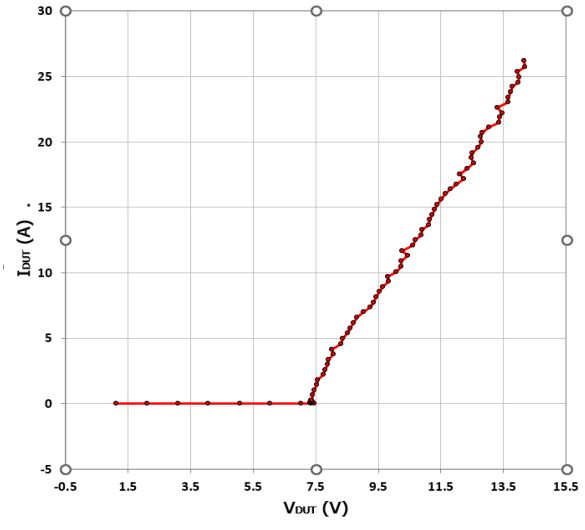


Fig. 17 DX TLP Curve Unpowered

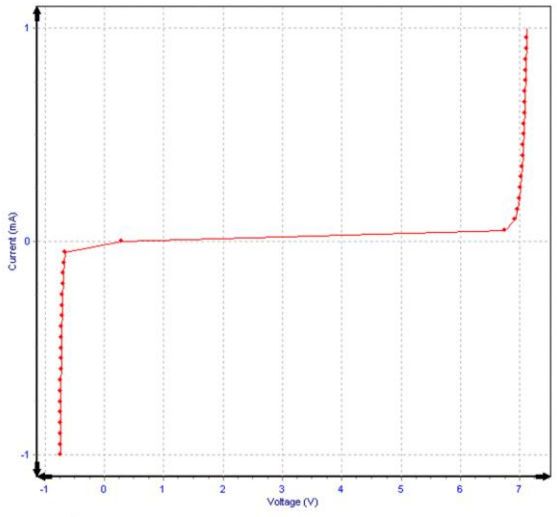


Fig. 18 DX IV Curve

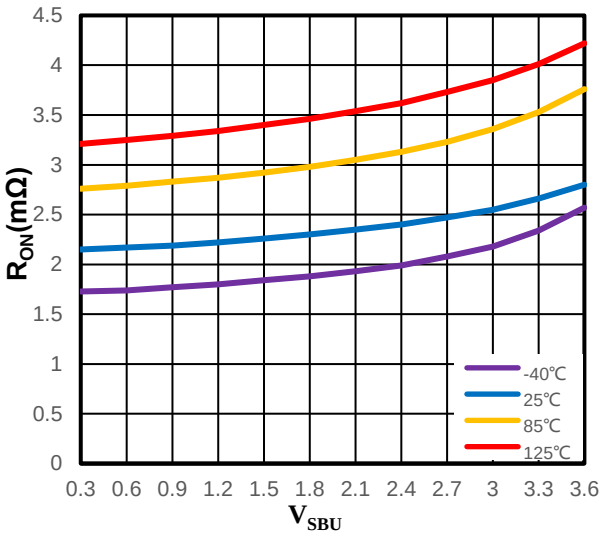


Fig. 19 SBU RON Flatness

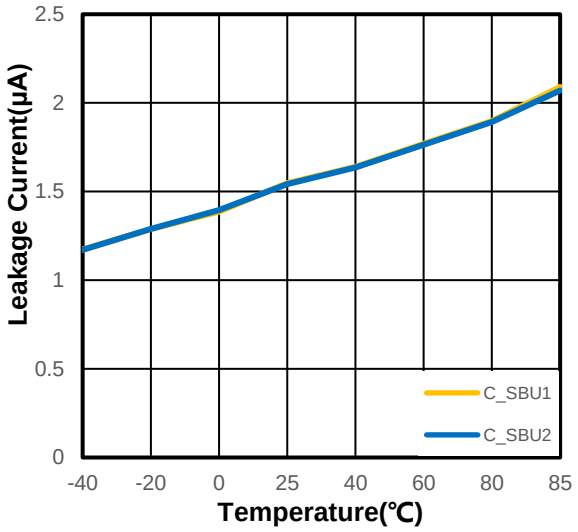


Fig. 20 SBU Path Leakage Current vs Ambient Temperature at 3.6 V

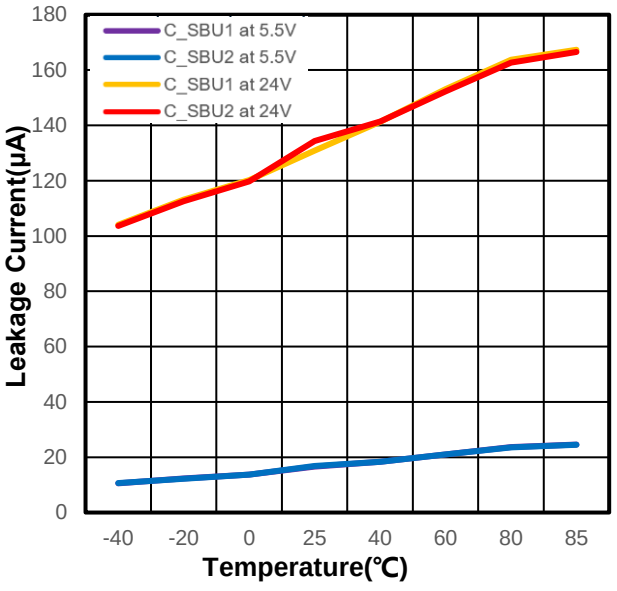


Fig. 21 C_SBU OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V

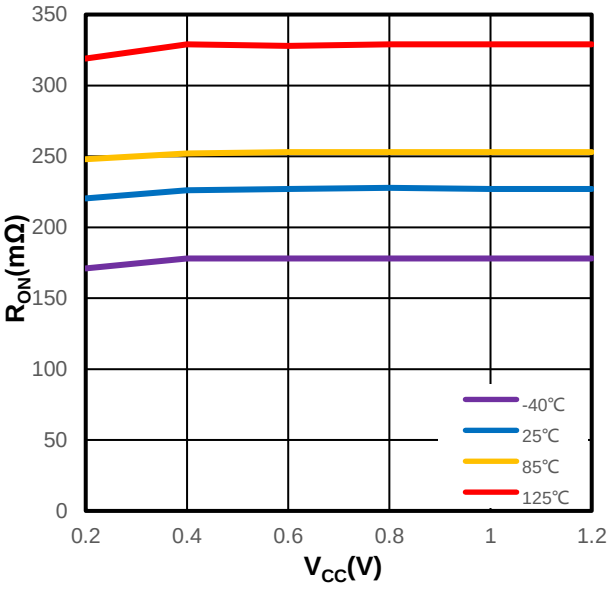


Fig. 22 CC RON Flatness

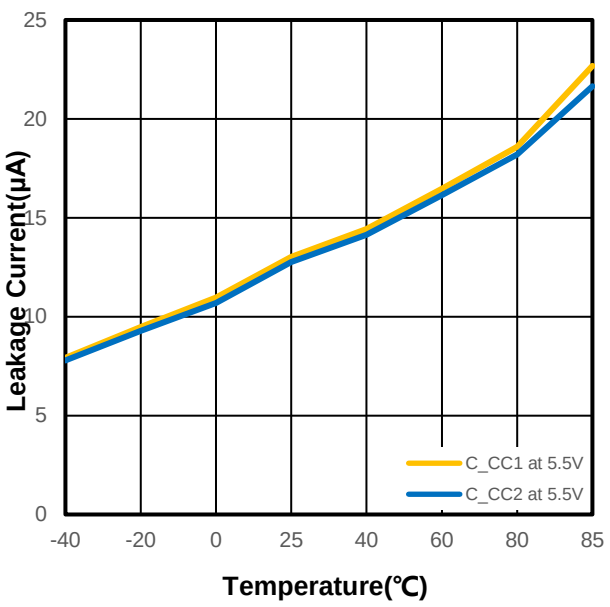


Fig. 23 C_CC Path Leakage Current vs Ambient Temperature at C_CC = 5.5 V

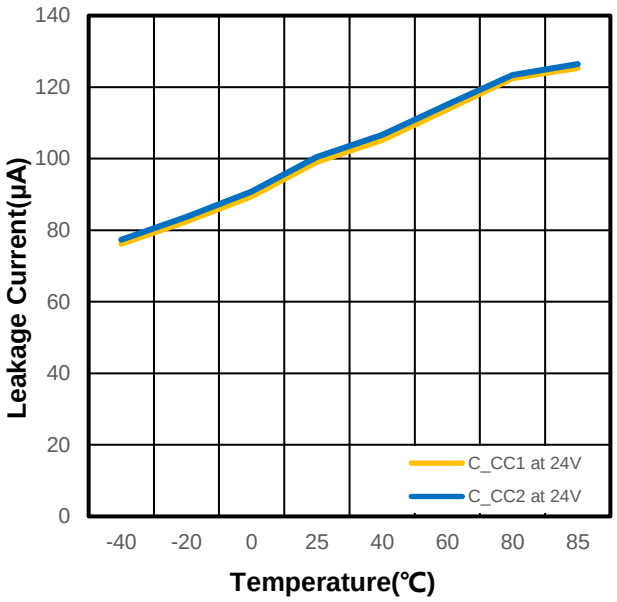


Fig. 24 C_CC Path Leakage Current vs Ambient Temperature at C_CC = 24 V

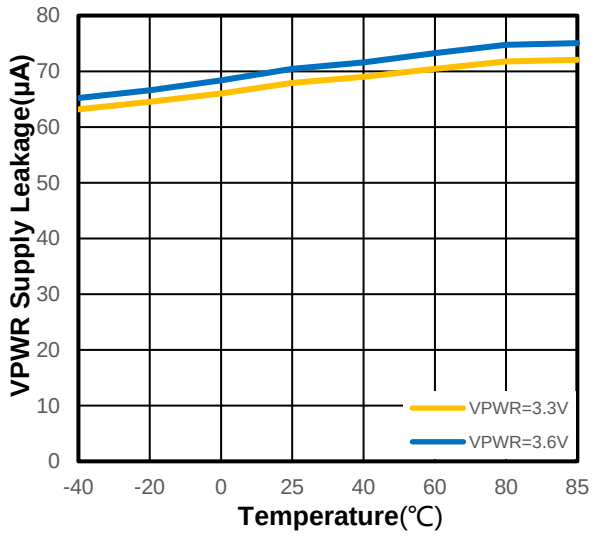


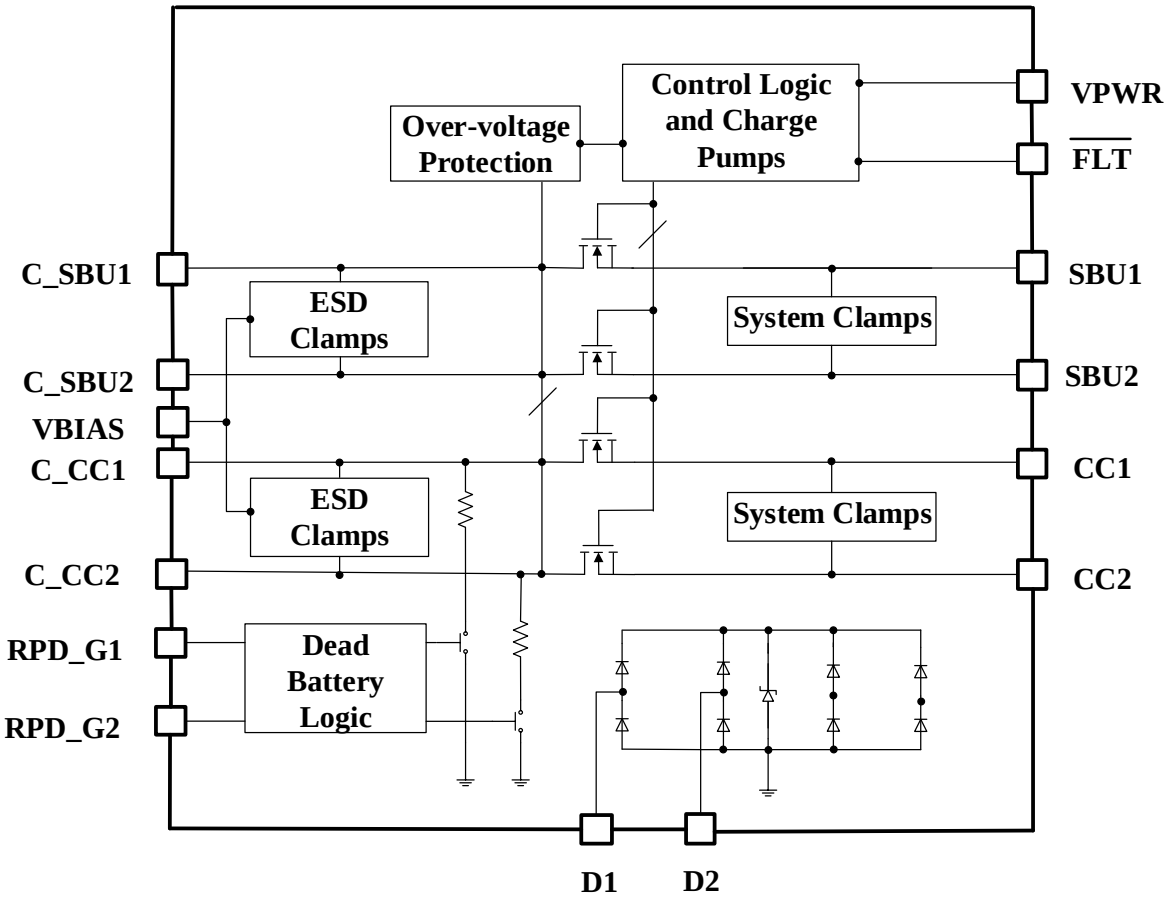
Fig. 25 VPWR Supply Leakage vs Ambient Temperature at 3.3V and 3.6V

13. Function Description

13.1 Overview

The WP5602 is a USB Type-C port protection chip that integrates four channels of 20-V Short-to-VBUS overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins and six channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, SBU2, DP, DM pins of the USB Type-C connector.

13.2 Block Diagram



13.3 Feature Description

13.3.1 4-Channels of Short-to-VBUS Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins): 24-V_{DC} Tolerant

The WP5602 provides 4-channels of Short-to-VBUS Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. The WP5602 is able to handle 24-V_{DC} on its C_CC1, C_CC2, C_SBU1, and C_SBU2 pins. This is necessary because according to the USB PD specification, with VBUS set for 20-V operation, the VBUS voltage is allowed to legally swing up to 21 V, and 21.5 V on voltage transitions from a different USB PD VBUS voltage.

13.3.2 6-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2, DP, DM Pins)

The WP5602 integrates 6-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2, DP, DM pins.

USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users.

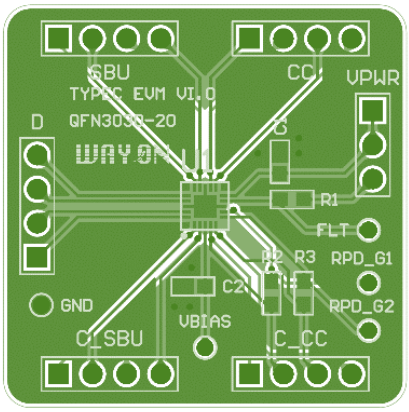
13.3.3 Dead-battery Mode

The WP5602 integrates high voltage dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection. If dead battery support is required, short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin. This connects the dead battery resistors to the connector CC pins.

14. Layout

For best performance, place the bypass capacitors as close as possible to the VPWR pin, and ESD protection capacitor as close as possible to the V_{BIAS} pin. The USB2.0 and SBU lines must be routed as straight as possible and any sharp bends must be minimized.

14.1 Layout Example



15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us to get the evaluation module or schematic.

The module names are listed in the table below.

NAME	PACKAGE	EVALUATION MODULE
WP5602	QFN3×3-20	TYPEC EVM V1.0 QFN3030-20

16. Naming Conventions

WP AB CC-DDD E

WP: WAYON Protection IC;

A: Product Category –5: Type C Protection;

B: Number of Protection Channels –6: 6 Channels;

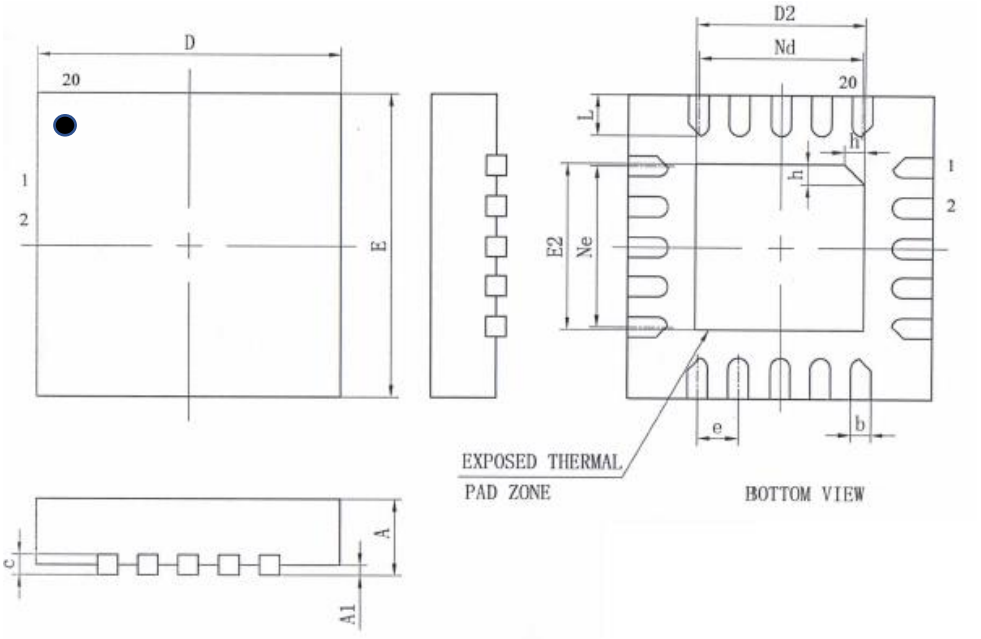
CC: Serial Number;

DDD: Package – Q3G: QFN3×3-20;

E: R-Reel & T-tube;

17. Package Information

QFN3×3-20



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60 BSC		
ND	1.60 BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F MIL	75*75		

18. Ordering Information

PART NUMBER	PACKAGE	PACKING QUANTITY	MARKING*
WP5602-Q3GR	QFN3×3-20	3k/Reel	WP5602 XXXX

* XXXX is variable.

Contact Information

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WAYON website: http://www.way-on.com
For additional information, please contact your local Sales Representative.
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Specifications are subject to change without notice.
The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

Product Specification Statement

- The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.
- The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. WAYON shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and WAYON assumes no responsibility for the application of the product.
- WAYON strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, WAYON cannot guarantee that the information provided in the product specification is entirely accurate and error-free. WAYON shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications. WAYON reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with WAYON to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult WAYON in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.
- Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.
- The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. WAYON shall assume no responsibility for any consequences resulting from such usage.
- Users should also comply with relevant laws, regulations, policies, and standards when using the product specification. Users are responsible for the risks and liabilities arising from the use of the product specification and must ensure that it is not used for illegal purposes. Additionally, users should respect the intellectual property rights related to the product specification and refrain from infringing upon any third-party legal rights. WAYON shall assume no responsibility for any disputes or controversies arising from the above-mentioned issues in any form.