WR3006

3A, Ultra-Low Dropout LDO

1. General Description

The WR3006 is an adjustable output voltage, low dropout CMOS Linear regulator with POK function. The WR3006 needs two supply voltages, one is a bias voltage (VDD) for internal control circuitry, the other is a main supply voltage (V_{IN}) for power conversion, to reduce power dissipation and provide extremely low dropout voltage.

The WR3006 can source 3A of output current with Low-dropout voltage and low quiescent current which make this series of devices ideal for battery-operated handheld equipments. The WR3006 has the fold-back maximum output current which depends on the output voltage. So the current limit functions both as a short circuit protection and as an output current limiter.

The WR3006 regulators are available in Green DFN3*3-10, ESOP-8 packages.

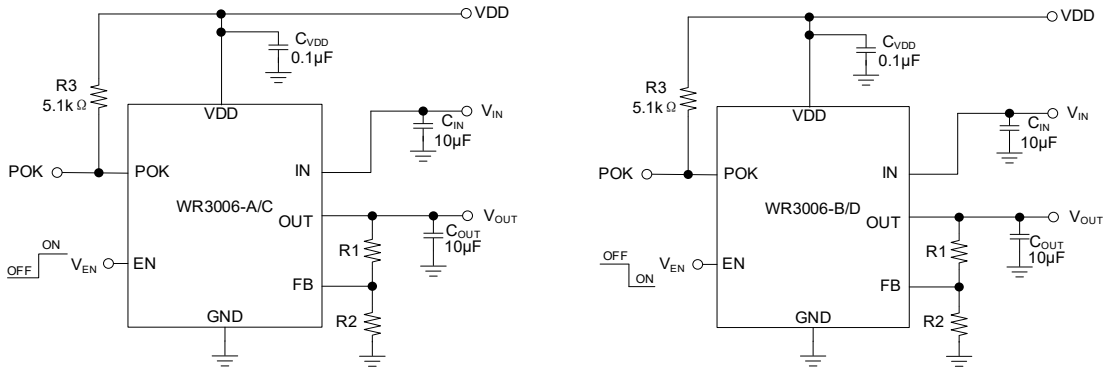
2. Features

- V_{IN} Input Voltage Range: 1.2V~5.5V
- VDD Input Voltage Range: 3.0V~5.5V
- Adjustable Output Voltage Range: 0.8V~(V_{IN}-V_{DROP}), (when V_{DD}-V_{OUT}>1.9V)
- Output Current: 3A
- High Output Accuracy: ±1.5%
- PSRR: 60dB@1kHz
- Dropout Voltage: 150mV @V_{OUT}=1.2V, I_{OUT} = 3A
- VDD Quiescent Current: 100μA (Typical)
- VIN Shut-down Current: < 1μA
- VDD Shut-down Current: < 3μA
- Operating Temperature: -40~+85℃
- Built-In Fold Back Protection Circuit
- Shutdown/Enable Control Function

3. Applications

- Front Side Bus VTT(1.2V/3A)
- Note Book PC Applications
- Motherboard Applications

4. Typical Application Circuit

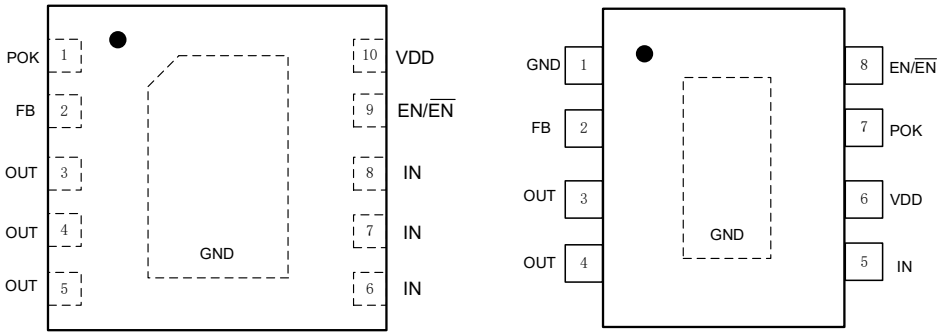


$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Figure. Adjustable Voltage Regulator

5. Pin Configuration

(Top View)



DFN3*3-10 **ESOP-8**

6. Pin Description

PIN NUMBER		PIN NAME	I/O	PIN FUNCTION
DFN3*3-10	ESOP-8			
1	7	POK	O	Power-OK signal output. This pin is an open-drain output used to indicate the status of output voltage within the Power-OK voltage window.
2	2	FB		Adjustable output voltage feedback input. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.
3,4,5	3,4	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 10μF, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible.
6,7,8	5	IN	I	Input voltage supply. Bypass with a typical 10μF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.
9	8	EN/$\overline{EN}$	I	Enable input. Active High for WR3006-A/C. Active Low for WR3006-B/D. EN is pulled up by a current source of 4μA for WR3006-A/D. EN is pulled down by a current source of 4μA for WR3006-B/C.
10	6	VDD	I	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended).
Exposed Pad	1	GND		Common ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

7. Absolute Maximum Ratings

Operating free-air temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{IN}	IN Input Voltage range		-0.3	-	6.0	V
V_{DD}	VDD Input Voltage range		-0.3	-	6.0	V
V_{EN}	EN Input Voltage range		-0.3	-	V_{DD}+0.3	V
V_{OUT}	Output Voltage range		-0.3	-	V_{IN}+0.3	V
V_{POK}	POK to GND Voltage		-0.3	-	6.0	V
V_{FB}	FB to GND Voltage		-0.3	-	V_{DD}+0.3	V
$I_{OUT(MAX)}$	Maximum output current		-	-	6.0	A
P_D	Power Dissipation, $P_{D(max)}$@T_A=25°C		-	-	1.8	W
$R_{\theta JA}$	Thermal resistance[2] [4]	ESOP-8	-	50	-	℃/W
		DFN3*3-10	-	50	-	℃/W
$R_{\theta JC}$	Thermal resistance[2] [3]	ESOP-8	-	18	-	℃/W
T_J	Maximum Junction Temperature		-	150	-	℃
T_{STG}	Storage Temperature		-65	-	150	℃
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		-	260	-	℃
ESD	HBM		-	4000	-	V

NOTE1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE2: Measured on 2cm x 2cm 2-layer FR4 PCB board, 1 oz copper, no via holes on GND copper.

NOTE3: Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

NOTE4: Power dissipation is calculate by $P_{D(MAX)} = (T_J - T_A) / R_{\theta JA}$.

8. Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{IN}	IN Input Voltage range		1.2	-	5.5	V
V_{DD}	VDD Input Voltage range		3.0	-	5.5	V
V_{EN}	EN Input Voltage range		0	-	5.5	V
V_{OUT}	Output Voltage range (When V_{DD}-V_{OUT}>1.9V)		0.8	-	V_{IN} - V_{DROP}	V
I_{OUT}	V_{OUT} Output Current	Continuous Current	0	-	3	A
		Peak Current	0	-	4	
C_{IN}	Input Capacitor		10	-	-	μF
C_{OUT}	Output Capacitor	V_{OUT}<1.4V	22	-	1100	μF
		V_{OUT}≥1.4V	10	-	1100	μF
C_{VDD}	VDD Capacitor		-	0.1	-	μF
$ESRC_{OUT}$	ESR of output Capacitor		0	-	200	mΩ
T_A	Operating Ambient temperature		-40	-	85	°C
T_J	Operating Junction temperature		-40	-	125	°C

9. Electrical Characteristics

(V_{DD} = 5V, V_{IN} = 1.8V, V_{OUT}=1.2V, I_{OUT}=1mA, C_{IN}=C_{OUT}=10μF, Enabled, T_A=25℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
SUPPLY CURRENT							
I_{VDD}	V_{DD} Supply Current	Enabled, I_{OUT}=0A			100	120	μA
I_{SD}	V_{DD} Supply Current at Shutdown	Disabled				3	μA
	V_{IN} Supply Current at Shutdown	Disabled				1	μA
POWER-ON-RESET (POR)							
V_{DDH}	Rising V_{DD} POR Threshold	V_{DD} Rising			2.7		V
Hysteresis	V_{DD} POR Hysteresis				0.1		V
V_{UVLO}	Rising V_{IN} POR Threshold	V_{IN} Rising		0.8	0.9	1.0	V
Hysteresis	V_{IN} POR Hysteresis				0.5		V
OUTPUT VOLTAGE							
V_{REF}	Reference Voltage	FB=V_{OUT}			0.8		V
V_{OUT}	Output Voltage Accuracy	V_{DD}=3.0 ~ 5.5V, I_{OUT}= 0~3A		-1.5		+1.5	%
LDR	Load Regulation	I_{OUT}=0A ~3A			3		mV
LNR	Line Regulation	I_{OUT}=10mA, V_{DD}= 3.0 ~ 5.5V		-0.15		+0.15	%/V
R_{DIS}	V_{OUT} Pull-low Resistance	V_{DD}=5V, Disabled, V_{OUT}<0.8V			85		Ω
I_{FB}	FB Input Current	V_{FB}=0.8V		-100		100	nA
DROPOUT VOLTAGE							
V_{DROP}	V_{IN}-to-V_{OUT} Dropout Voltage	V_{DD}=5.0V, I_{OUT}=3A	V_{OUT}=1.2V		0.15	0.28	V
			V_{OUT}=1.8V		0.16	0.29	
			V_{OUT}=2.5V		0.19	0.31	
I_{LIM}	Current-Limit Level				5.5		A

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
PROTECTIONS						
I_{SHORT}	Short Current-Limit Level	V_{FB}<0.2V		1.2		A
	Short Current-Limit Blanking Time	From beginning of soft-start		0.6		ms
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		50		°C
ENABLE AND SOFT-START						
V_{ENH}	EN Logic High Threshold Voltage	V_{EN} rising	0.5	0.8	1.1	V
hysteresis	EN Hysteresis			0.1		V
I_{EN}	EN Pull-Low Current	Enabled		4		μA
t_{SS}	Soft-Start Interval	V_{OUT}=10% to 90%		0.3		ms
t_{ON}	Turn On Delay	From being enabled to V_{OUT} rising 10%		180		μs
POWER-OK AND DELAY						
V_{THPOK}	Rising POK Threshold Voltage	V_{FB} rising		94		%
	POK Threshold Hysteresis	V_{FB} falling		8		%
	POK Pull-low Voltage	POK sinks 5mA		0.25	0.4	V
	POK Debounce Interval	V_{FB}<falling POK voltage threshold		15		μs
	POK Delay Time	From V_{FB} =V_{THPOK} to rising edge of the V_{POK}	1	2	4	ms

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
Power Supply Rejection Ratio							
$PSRR_V_{IN}$	Power Supply Rejection Ratio	$V_{IN} \geq V_{OUT}$ + 0.5V, V_{DD} =5V, V_{IN} to V_{OUT}, I_{OUT} = 10mA,	f=100Hz		75		dB
			f=1kHz		65		dB
			f=10kHz		45		dB
$PSRR_V_{DD}$	Power Supply Rejection Ratio	$V_{IN} \geq V_{OUT}$ + 0.5V, V_{DD} =5V, V_{DD} to V_{OUT}, I_{OUT} = 10mA,	f=100Hz		70		dB
			f=1kHz		60		dB
			f=10kHz		40		dB

10. Typical Performance Characteristics

(V_{DD} = 5V, V_{IN} = 1.8V, V_{OUT}=1.2V, I_{OUT}=1mA, C_{IN}=C_{OUT}=10μF, Enabled, T_A=25°C, unless otherwise noted)

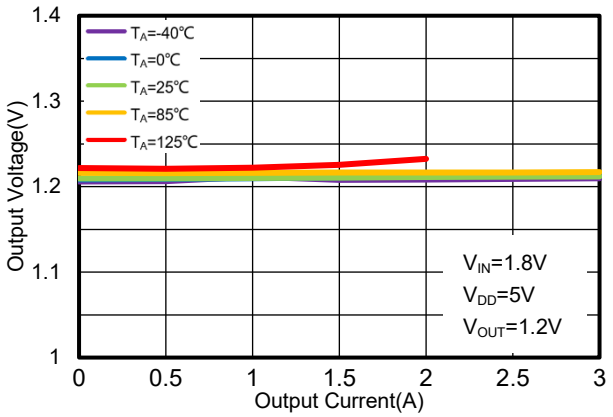


Figure 1. WR3006-CFEAR
Load Regulation vs. I_{OUT} & Ambient Temperature

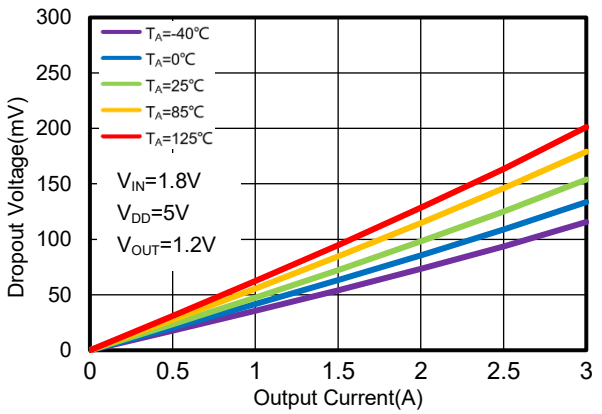


Figure 2. WR3006-CFEAR
Dropout Voltage vs. I_{OUT} & Ambient Temperature

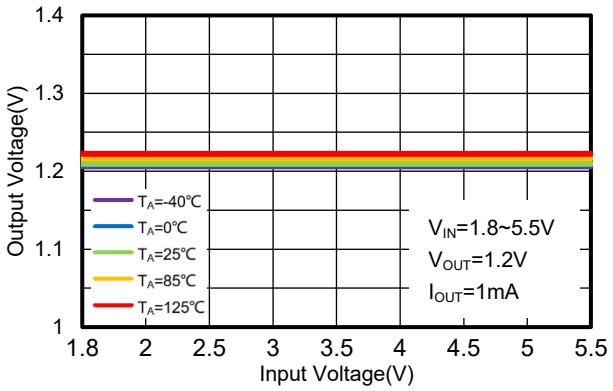


Figure 3. WR3006-CFEAR
Regulation vs. V_{IN} (Line Regulation) & Ambient Temperature

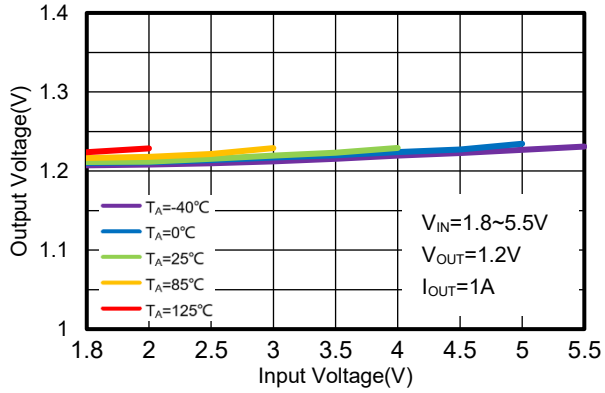


Figure 4. WR3006-CFEAR
Regulation vs. V_{IN} (Line Regulation) & Ambient Temperature

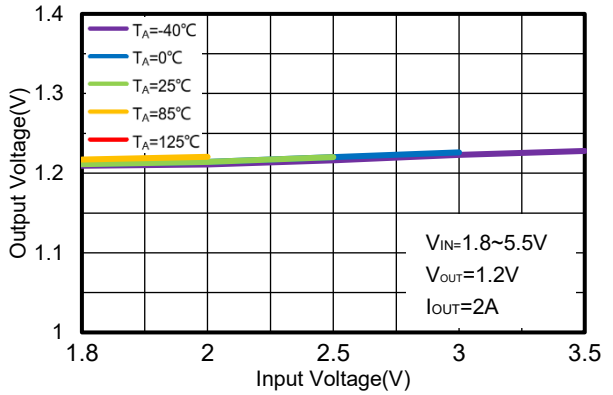


Figure 5. WR3006-CFEAR
Regulation vs. V_{IN} (Line Regulation) & Ambient Temperature

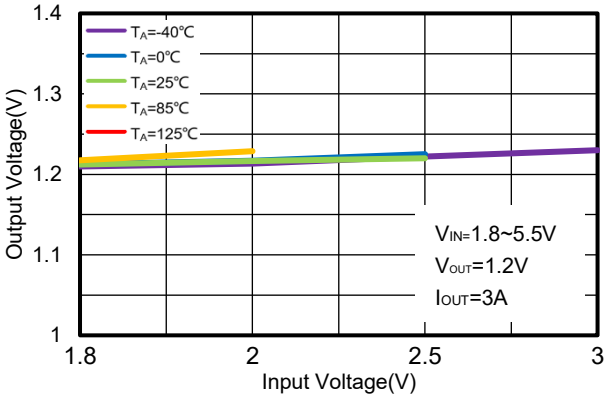


Figure 6. WR3006-CFEAR
Regulation vs. V_{IN} (Line Regulation) & Ambient Temperature

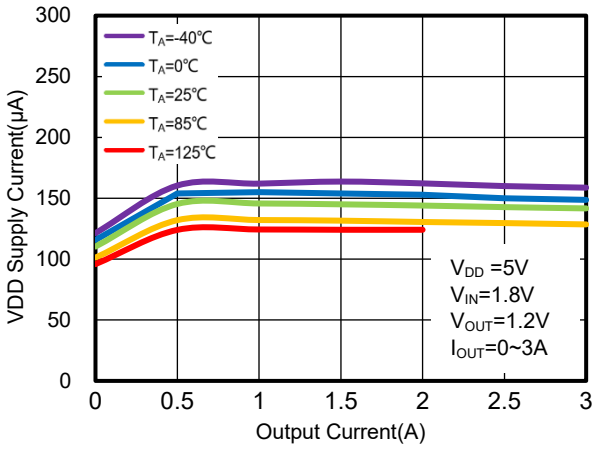


Figure 7. WR3006-CFEAR
VDD Supply Current vs. I_{OUT} & Ambient Temperature

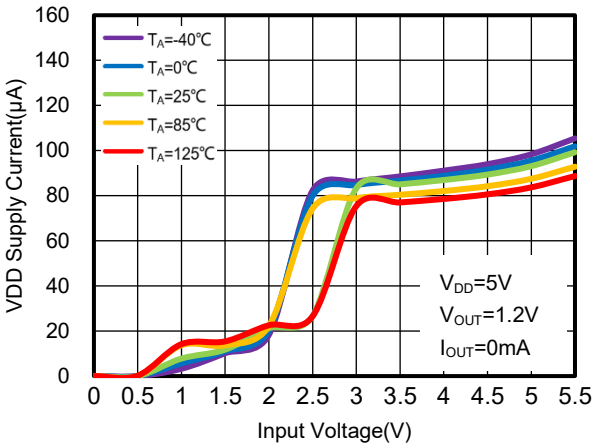


Figure 8. WR3006-CFEAR
VDD Supply Current vs. V_{IN} & Ambient Temperature

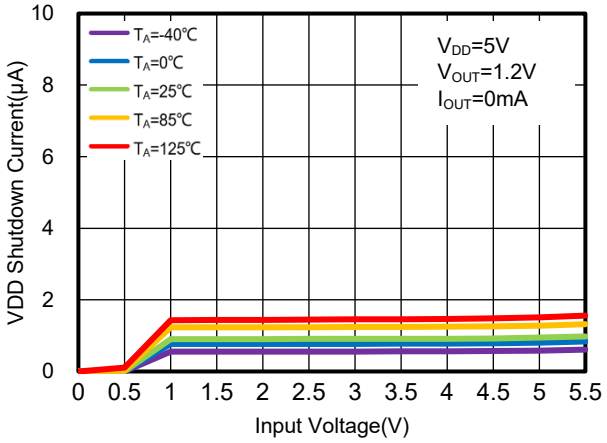


Figure 9. WR3006-CFEAR
VDD Shutdown Current vs. V_{IN} & Ambient Temperature

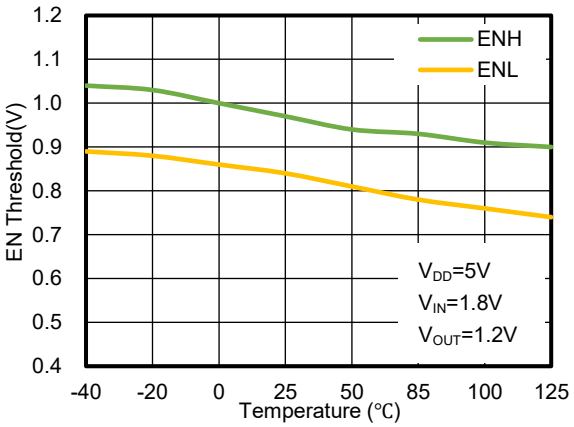


Figure 10. WR3006-CFEAR
Enable Threshold vs. Ambient Temperature

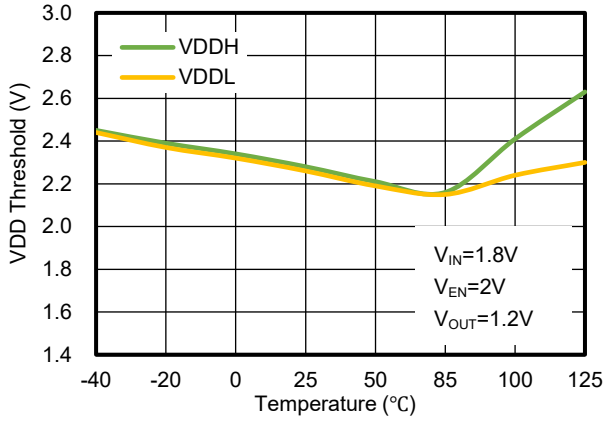


Figure 11. WR3006-CFEAR
VDD Threshold vs. I_{OUT} & Ambient Temperature

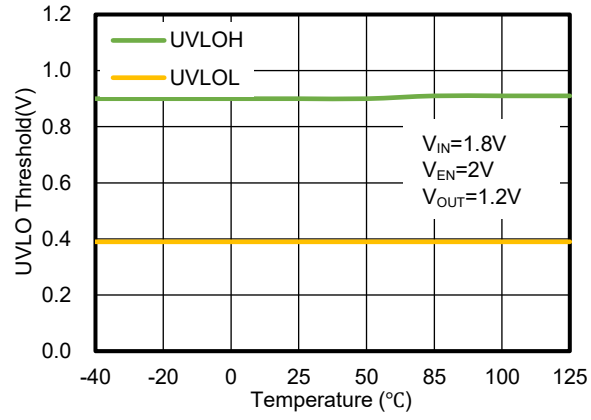


Figure 12. WR3006-CFEAR
UVLO Threshold vs. I_{OUT} & Ambient Temperature

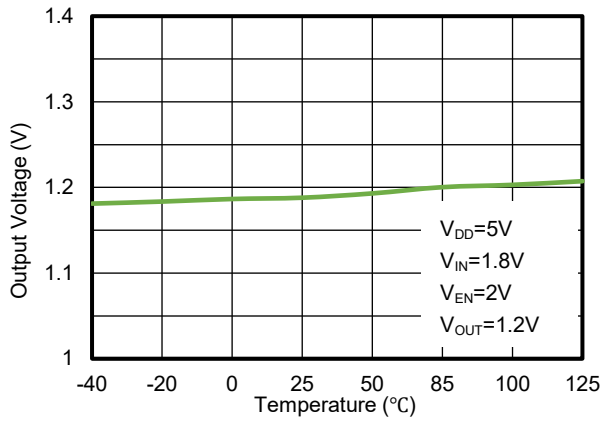


Figure 13. WR3006-CFEAR
Output Voltage vs. Ambient Temperature

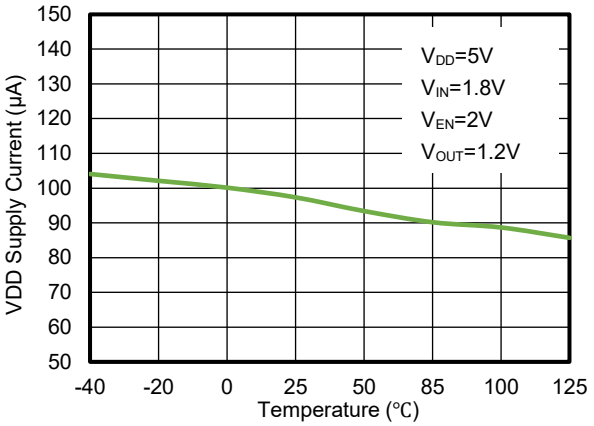


Figure 14. WR3006-CFEAR
VDD Supply Current vs. Ambient Temperature

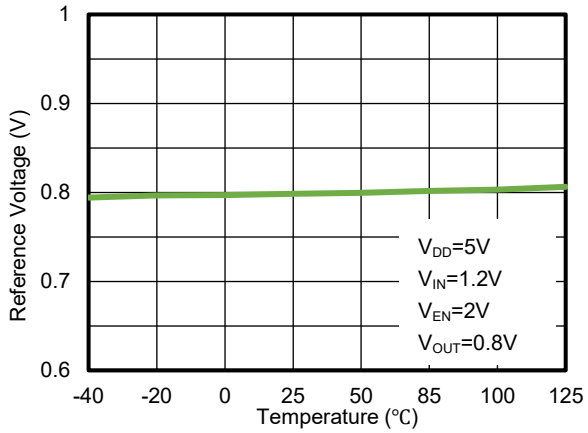


Figure 15. WR3006-CFEAR
Reference Voltage vs. Ambient Temperature

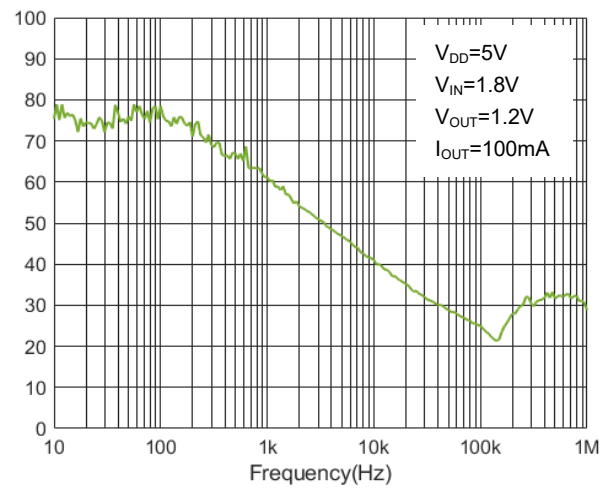


Figure 16. WR3006-CFEAR
VDD Power Supply Rejection Ratio vs. Frequency

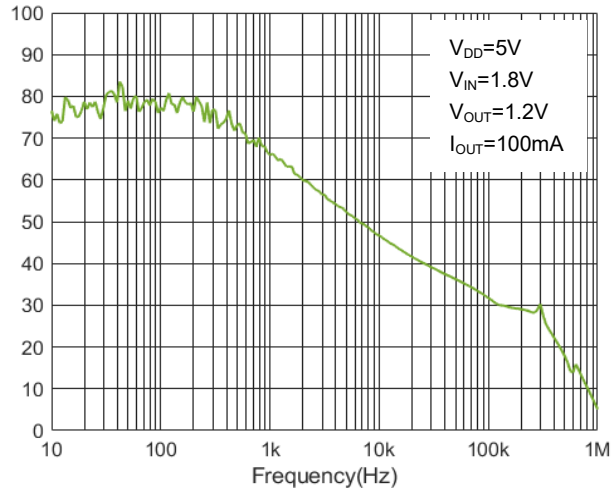


Figure 17. WR3006-CFEAR
V_{IN} Power Supply Rejection Ratio vs. Frequency

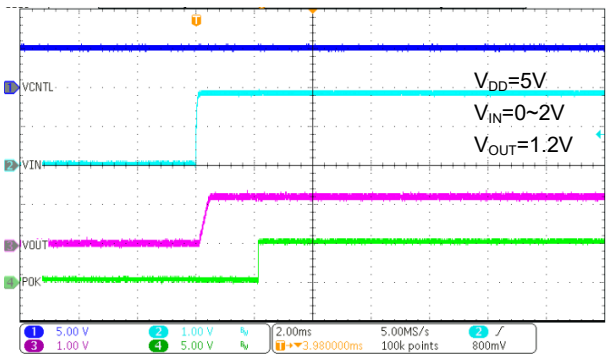


Figure 18. WR3006-CFEAR
Power On

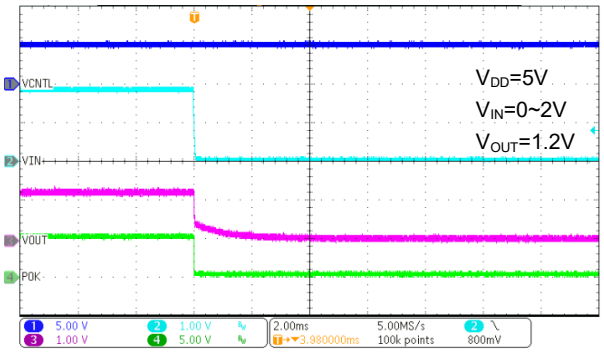


Figure 19. WR3006-CFEAR
Power Off

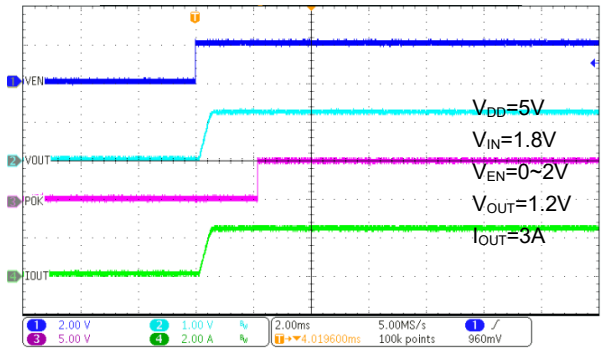


Figure 20. WR3006-CFEAR
Soft Start from EN

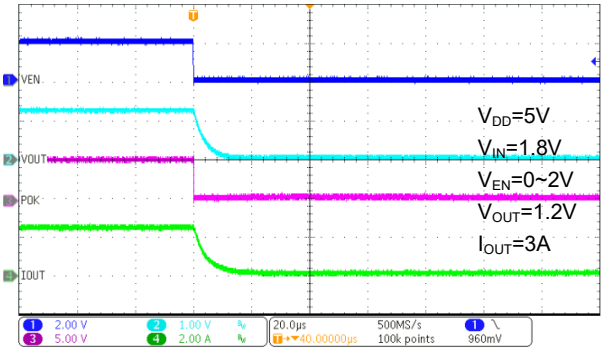


Figure 21. WR3006-CFEAR
EN Shutdown

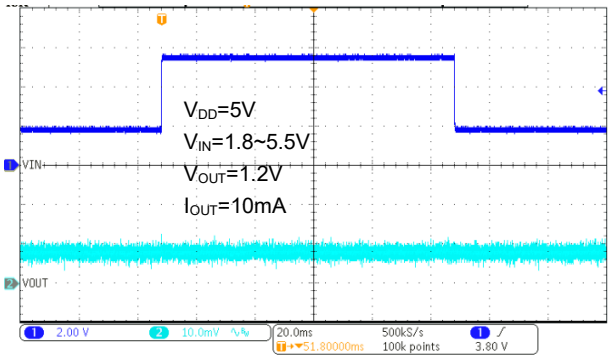


Figure 22. WR3006-CFEAR
Line Transient

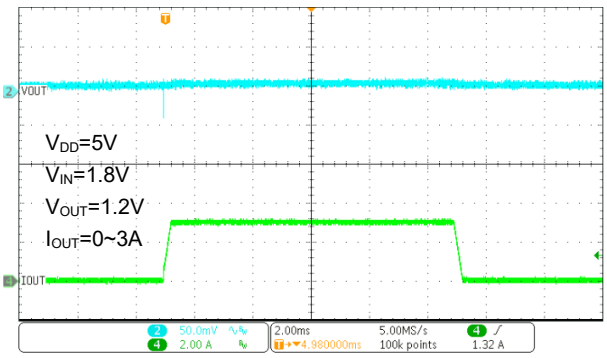


Figure 23. WR3006-CFEAR
Load Transient

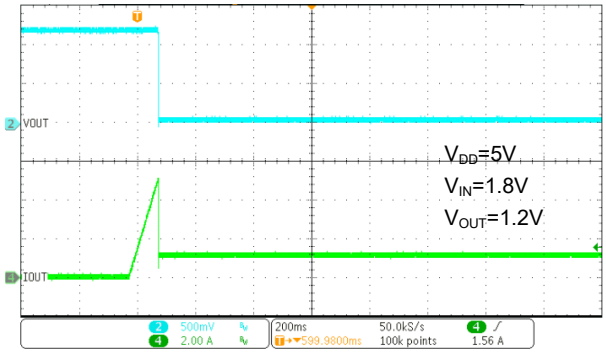


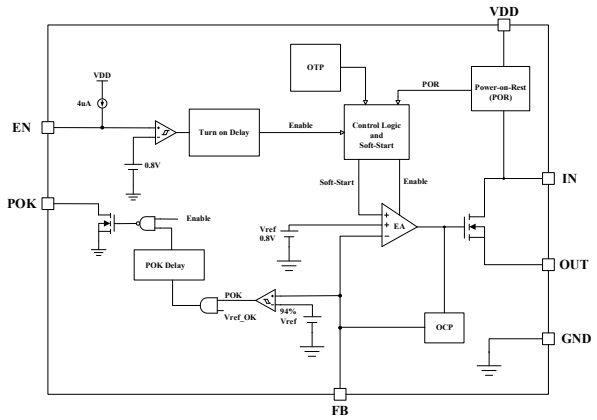
Figure 24. WR3006-CFEAR
Over Current Protection

11. Function Description

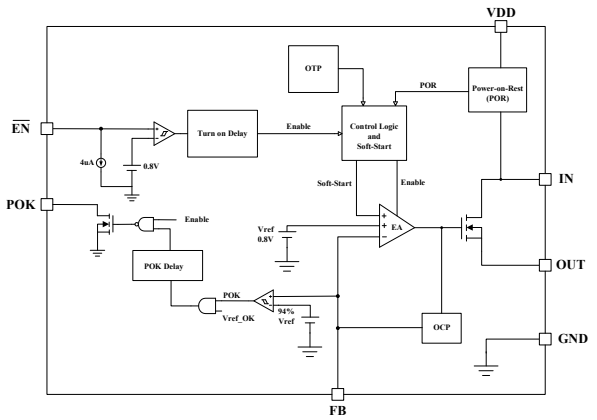
11.1 Overview

The WR3006 is a 3A linear regulator with adjustable output, which needs two supply voltages to reduce power dissipation and provide extremely low dropout voltage It features foldback current limiting and Power-OK indication. The WR3006 is designed to be used in a variety of applications.

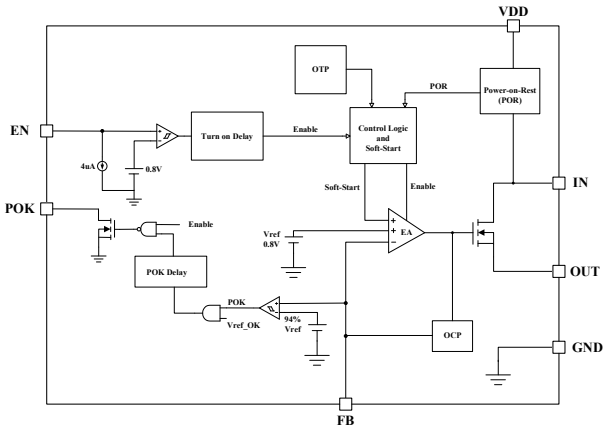
11.2 Block Diagram



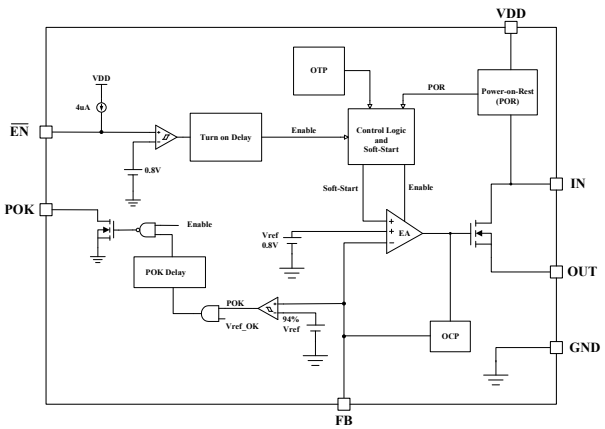
Version: WR3006-A.



Version: WR3006-B.



Version: WR3006-C.



Version: WR3006-D.

11.3 Feature Description

11.3.1 Output Voltage Accuracy

Output voltage accuracy is defined as the maximum and minimum error in output voltage. The errors are introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots. The output voltage accuracy of WR3006 is about 1.5% at T_A = 25℃ and maybe drift in full operating temperature.

11.3.2 Enable (EN)

The EN of WR3006-A/D is pulled up by a current source of 4μA. The EN of WR3006-B/C is pulled down by a current source of 4μA. When the EN input voltage of WR3006-A/C is higher than the high enable voltage threshold, the device outputs normally. When the EN input voltage of WR3006-B/D is lower than the low enable voltage threshold, the device outputs normally.

VERSION	EN=HIGH	EN=LOW	EN FLOATING
A	enable	disable	enable
B	disable	enable	enable
C	enable	disable	disable
D	disable	enable	disable

11.3.3 Dropout Voltage (VDO)

WR3006 is a low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the minimum of (V_{IN}-V_{OUT}) at the rated maximum output current where V_{OUT} is the minimum of $V_{OUT(NOM)}$. When the input voltage is below $V_{OUT(NOM)}$ plus VDO, the output voltage varies with the input voltage.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS\ (ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The $R_{DS\ (ON)}$ is calculated by following equation.

$$R_{DS\ (ON)}=V_{DO}/I_{OUT}$$

11.3.4 Power Supply Rejection Ratio (PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$PSRR = 20lg\ (Ripple(in) / Ripple(out))$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

11.3.5 Foldback Current Limit (I_{LIM})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{LIM}, and when an overload or short circuit occurs, the output current will be maintained at I_{LIM}, and the output voltage will be reduced to $I_{LIM}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{LIM}. The output current is reduced to the set current threshold I_{SHORT} and the output voltage is reduced to $I_{SHORT}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

The WR3006 uses a foldback current limiting mode where the final current is clamped to around 1.2A, thus providing good protection to the device.

11.3.6 Power-On-Reset

A Power-On-Reset (POR) circuit monitors both of supply voltages on VDD and IN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on. The POR function also pulls low the POK voltage regardless the output status when one of the supply voltages falls below its falling POR voltage threshold.

11.3.7 Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge during start-up. The typical soft-start interval is about 0.3ms.

11.3.8 Thermal Protection

The WR3006 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 160°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 110°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR3006's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR3006 into a thermal shutdown state will reduce the reliability of the device.

11.3.9 Power-OK and Delay

The WR3006 indicates the status of the output voltage by monitoring the feedback voltage (V_{FB}) on FB pin. As the V_{FB} rises and reaches the rising Power-OK voltage threshold (V_{THPOK}), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate that the output is ok. As the V_{FB} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 15μs typical).

11.4 Functional Mode of The Device

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS				
	V_{IN}	V_{DD}	V_{EN}	I_{OUT}	T_J
Normal	5.5V>V_{IN} >$V_{OUT(NOM)}$ + V_{DROP_IN}	5.5V>V_{DD}>3.0V, (V_{DD}-V_{OUT}>1.9V)	Enable	I_{OUT} < I_{LIM}	T_J < T_{SD}
Dropout	V_{IN} < $V_{OUT(NOM)}$ + V_{DROP_IN}	5.5V>V_{DD}>3.0V, (V_{DD}-V_{OUT}>1.9V)	Enable	I_{OUT} < I_{LIM}	T_J < T_{SD}
Disabled	V_{IN} < V_{UVLO}	V_{DD} < V_{DDH}	Disable	—	T_J > T_{SD}

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(NOM)}$ + V_{DROP_IN}) and is less than 5.5V.
2. The V_{DD} Input voltage is between 3.0V and 5.5V, and (V_{DD}-V_{OUT}>1.9V) is a must.

3. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.
4. The output current is less than the current limit ($I_{OUT} < I_{LIM}$).
5. The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, the device operates in the dropout state and the output voltage tracks the input voltage.

11.4.3 Disabled

The WR3006 can be turned off when EN disabled, the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application and Implementation

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR3006 is a linear voltage regulator with an input voltage of 1.2V to 5.5V and an output voltage of 0.8V to (V_{IN} - V_{DROP}). The accuracy is 1.5% for V_{REF} voltages. The maximum output current is 3A. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Capacitor Recommendation

The WR3006 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN}, V_{DD} and V_{OUT} pins to improve their stability. The use of multilayer ceramic capacitors is recommended. These capacitors also have limitations. Ceramic capacitors with X7R-, X5R- and COG grade dielectric materials have relatively good capacitive stability at different temperatures. The WR3006 is designed to use 10μF ceramic capacitors at the input, 0.1μF ceramic capacitors at VDD and 10μF or larger ceramic capacitors at the output. Place C_{IN}, C_{VDD} and C_{OUT} as close as possible to the IN, VDD and OUT pins to minimize the tracking inductance from the capacitors to the device.

12.1.2 Power Dissipation (P_D)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

P_D can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage. The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance ($R_{\theta JA}$) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

The thermal resistance ($R_{\theta JA}$) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.3 Detailed Design Procedure

The adjustable version of WR3006 has a thermally stable reference voltage of 0.8 ± 0.012V， the voltage on the FB pin sets the output voltage which is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Lower values for R1 and R2 is recommended to reduce the noise injected from the FB pin. Note that R1 is connected from OUT pin to FB pin, and R2 is connected from FB to GND.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right)$$

In order to get better load regulation, R1 must be connected very close to the OUT and FB pin, while the ground of R2 must be as close as possible to the ground pin of the chip.

Recommended Component Values

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
1.2	12	24
1.8	30	24
2.5	51	24
3.3	75	24

13. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us to get the evaluation module or schematic.

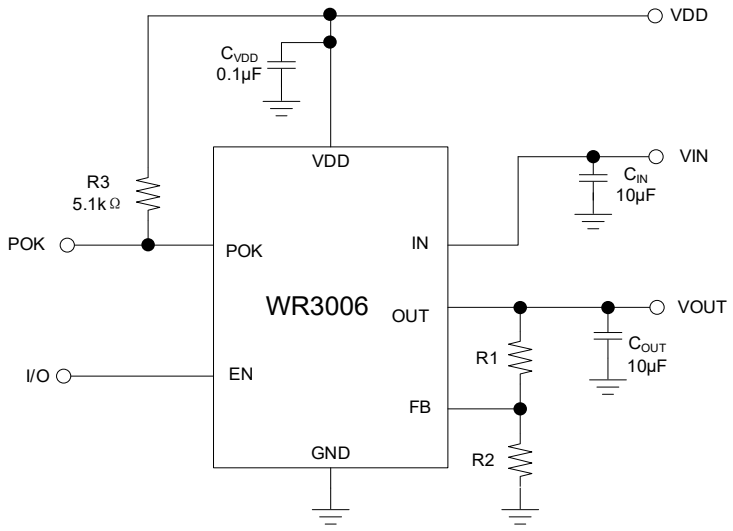
The module names are listed in the following table.

NAME	PACKAGE	EVALUATION MODULE
WR3006	ESOP-8	WAYON LDO EVM V1.0 – ESOP-8
	DFN3*3-10	WAYON LDO EVM V1.0 - DFN3*3-10

13.1 Schematic

The following figure shows the schematic of the application circuit.

Circuit schematic: EN is controlled by external voltage.



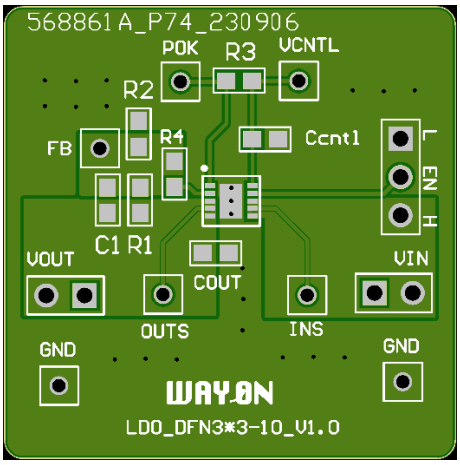
13.2 Layout of Typical Application Circuits

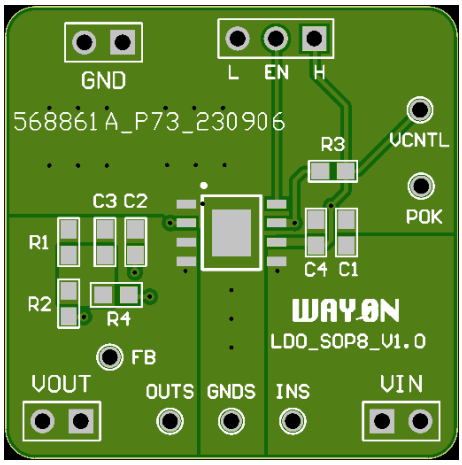
13.2.1 Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. A minimum 10μF input capacitor (C_{IN}) is recommended to IN to minimize the effect of resistance and inductance between the source and the LDO input. A minimum 0.1μF VDD input capacitor (C_{VDD}) is recommended to VDD and a minimum 10μF output capacitor (C_{OUT}) is recommended to OUT. Connect the ground sides of C_{IN}, and C_{OUT} with LDO ground pins as close as possible through a wide copper surface. Through-holes and long wires may seriously affect system performance and is not recommended.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

13.2.2 Layout Example





14. Naming Conventions

WR AA BB-X DDD E

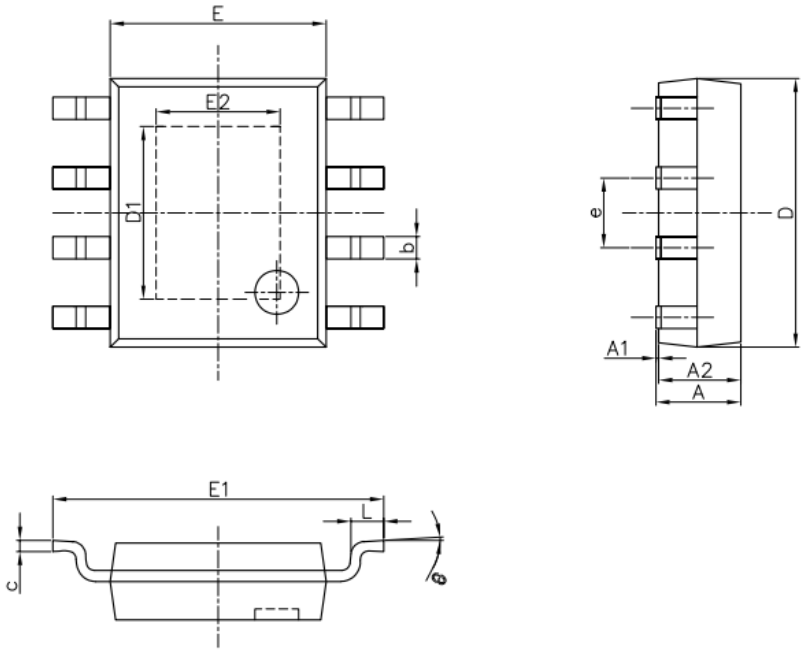
WR: WAYON Regulator;
AA: 30 –Output Current, 3A;
BB: Serial number;
X : A-Active High / Initial On
B-Active Low / Initial On
C-Active High / Initial Off
D-Active Low / Initial Off
DDD: Package – P80: ESOP-8
FEA: DFN3*3-10
E : R-Reel;

15. Electrostatic Discharge Warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

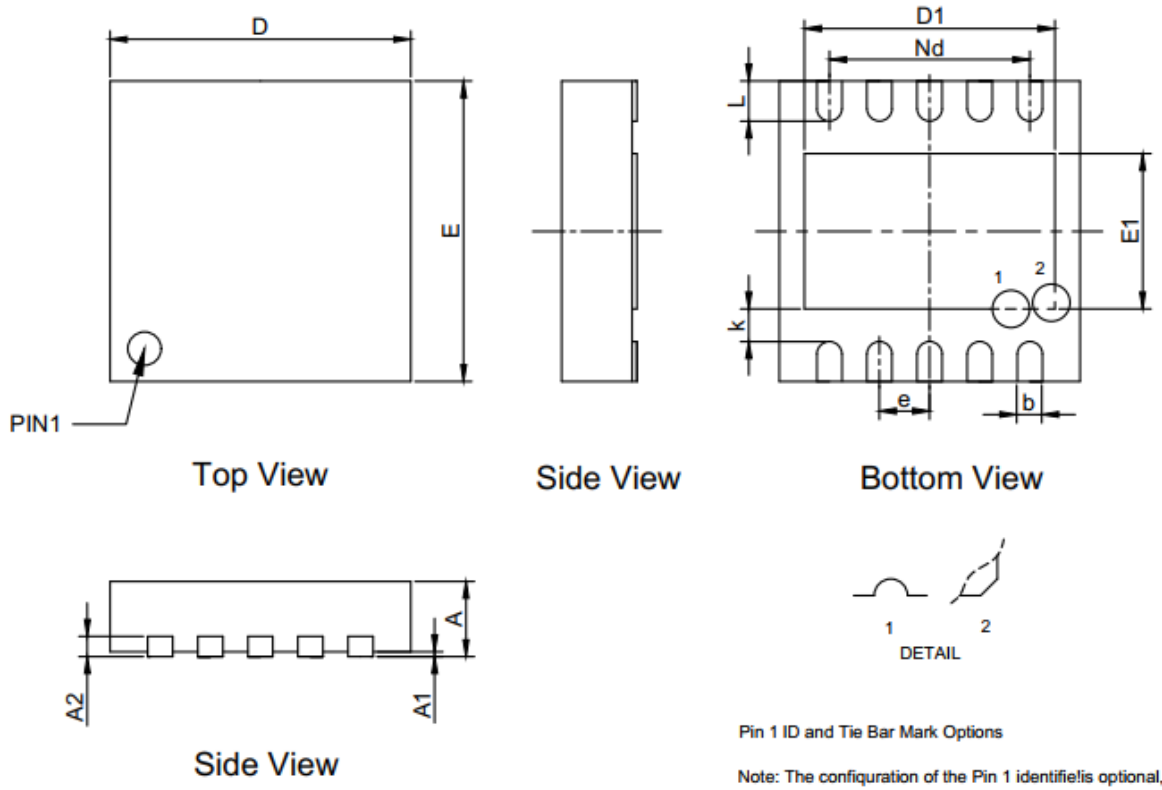
16. Package Information

ESOP-8



SYMBOL	DIMENSIONS IN MILLIMETERS	
	MIN	MAX
A	1.30	1.70
A1	0.00	0.18
A2	1.30	1.55
b	0.33	0.51
c	0.17	0.25
D	4.70	5.10
D1	2.00	3.50
E	3.70	4.10
E1	5.80	6.20
E2	2.00	2.50
e	1.270BSC	
L	0.40	1.27
θ	0°	8°

DFN3*3-10



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2		0.203REF	
b	0.15	0.25	0.35
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.20	-	2.60
E1	1.45	-	1.90
e		0.50BSC	
Nd		2.00BCS	
k	0.20	-	-
L	0.30	0.40	0.50

17. Ordering Information

PART NUMBER	INITIALSTATE	PACKAGE	PACKING QUANTITY	MARKING*
WR3006-AP80R	Active High/Initial On	ESOP-8	4k/Reel	WR3006 A XXXX
WR3006-BP80R	Active Low/Initial On	ESOP-8	4k/Reel	WR3006 B XXXX
WR3006-CP80R	Active High/Initial Off	ESOP-8	4k/Reel	WR3006 C XXXX
WR3006-DP80R	Active Low /Initial Off	ESOP-8	4k/Reel	WR3006 D XXXX
WR3006-AFEAR	Active High/Initial On	DFN3*3-10	3k/Reel	WR3006 A XXXX
WR3006-BFEAR	Active Low /Initial On	DFN3*3-10	3k/Reel	WR3006 B XXXX
WR3006-CFEAR	Active High/Initial Off	DFN3*3-10	3k/Reel	WR3006 C XXXX
WR3006-DFEAR	Active Low /Initial Off	DFN3*3-10	3k/Reel	WR3006 D XXXX

* XXXX is variable.

Contact Information

No.1001, Shiwan(7) Road, Pudong District, Shanghai, P.R.China.201207
Tel: 86-21-50310888 Fax: 86-21-50757680 Email: market@way-on.com
WAYON website: http://www.way-on.com
For additional information, please contact your local Sales Representative.
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Product Specification Statement

1.The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.

2.The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. WAYON shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and WAYON assumes no responsibility for the application of the product.

3.WAYON strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, WAYON cannot guarantee that the information provided in the product specification is entirely accurate and error-free. WAYON shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications. WAYON reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with WAYON to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult WAYON in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.

4.Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.

5.The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. WAYON shall assume no responsibility for any consequences resulting from such usage.

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