WR1006

Ultra low dropout, 500mA/1A, CMOS LDO

1. General Description

The WR1006 series are CMOS-based low-dropout, low-power linear regulators, offering 500mA/1A with low dropout voltage, high ripple rejection, high output accuracy and low supply current. The WR1006 series consist of an accurate voltage-reference block, an error amplifier, a voltage-setting resistor net, a PMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit with short protection.

The WR1006 series use a type of outstanding CMOS process to minimize the supply current. A low on-resistance PMOS pass device is equipped for lower dropout voltage. WR1006 also possess the EN function to save more energy and extend the battery life.

The WR1006 series can choose the output current between 500mA and 1A by setting the LCON pin to high or low.

The WR1006 series are available in the DFN1612-8 package.

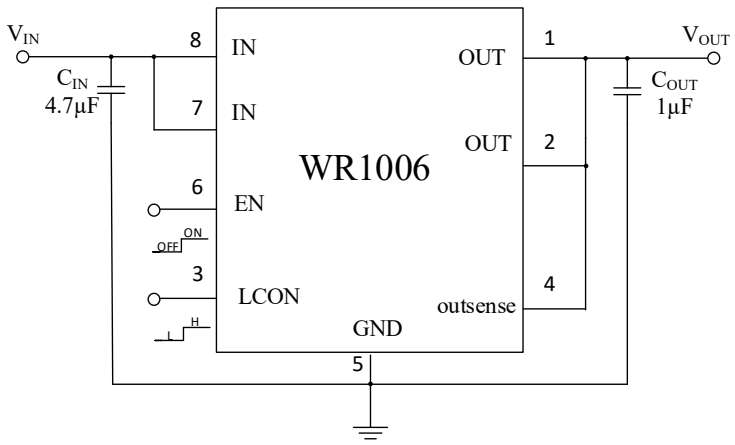
2. Features

- Wide Input Voltage Range: 2.5V to 5.5V
- Output Current: 500mA/1A optional
- Output Voltage Range: 1.0V to 3.3V
- Very Low IQ: 160μA
- Excellent Load/Line Transient Response
- Line Regulation: 0.02% typical
- Built-in over current protection and thermal shutdown circuit
- Built-in Start from EN Current Suppression Circuit and Current Limit
- Reverse Current Protection
- Built-in Auto-discharging circuit (optional)

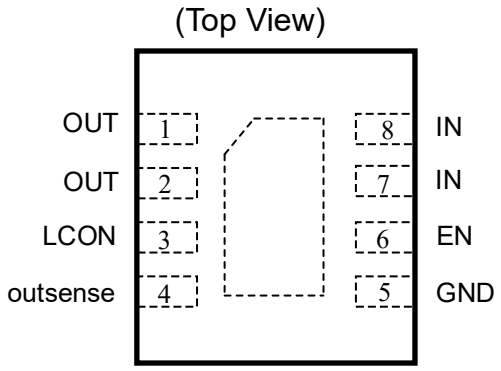
3. Applications

- Cellphones, radiophone, digital cameras
- Bluetooth, wireless handsets
- Others portable electronic device

4. Typical Application



5. Pin Configuration



DFN1612-8

6. Pin Description

PIN NUMBER	PIN NAME	I/O	PIN FUNCTION
1,2	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 4.7μF, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible.
3	LCON	I	Output Current Limit Alternate （“H”=1A，“L”=500mA）
4	outsense	O	Feedback
5	GND	-	Common ground.
6	EN	I	Enable input. Active High.
7,8	IN	I	Input voltage supply. Bypass with a typical 4.7μF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.

7. Absolute Maximum Ratings

Operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		RATING	UNIT
Input Voltage (IN Pin)		-0.3 to 6.0	V
Input Voltage (EN Pin)		-0.3 to 6.0	V
Input Voltage (LCON Pin)		-0.3 to 6.0	V
Output Voltage		-0.3 to 6.0	V
Power Dissipation[2][4], P_D @T_A = 25ºC	DFN1612-8	750	mW
Thermal Resistance[2][3], θ_{JA}	DFN1612-8	165	℃/W
Junction Temperature		150	℃
Lead Temperature Range		260	℃
Storage Temperature Range		-55 to 150	℃
ESD Susceptibility	HBM	±4000	V

NOTE1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE2: Measured on 2cm x 2cm 2-layer FR4 PCB board, 1oz copper, no via holes on GND copper.

NOTE3: Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

NOTE4: Power dissipation is calculated by $P_{D(MAX)} = T_J - T_A / R_{\theta JA}$.

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Input voltage range	2.5 to 5.5	V
EN Input voltage range	0 to 5.5	V
Nominal output voltage range	1.0 to 3.3	V
Output current	500/1000	mA
Input capacitor	4.7	μF
Output capacitor	1	μF
Operating temperature range	-40 to 85	℃

9. Electrical Characteristics

(T_A=25 ℃, V_{IN}=V_{OUT}+1.0V, I_{OUT}=1mA, C_{IN} =4.7μF, C_{OUT}=1μF, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
V_{OUT}	Output Voltage Range	V_{IN}=V_{OUT}+1.0V		0.98 V_{OUT}		1.02 V_{OUT}	V
V_{DO}	Dropout Voltage[5]	V_{OUT}=3.3V, I_{OUT}=500mA			65		mV
		V_{OUT}=3.3V, I_{OUT}=1A			130		
		V_{OUT}=3.0V, I_{OUT}=500mA			65		
		V_{OUT}=3.0V, I_{OUT}=1A			130		
		V_{OUT}=1.8V, I_{OUT}=500mA			250		
		V_{OUT}=1.8V, I_{OUT}=1A			300		
I_{OUT}	Output Current Limit	V_{IN}=V_{OUT}+0.5V	LCON="L"	500			mA
			LCON="H"	1000			
I_{SHORT}	Short Current Limit	V_{OUT}=0V	LCON="H"		160		mA
			LCON="L"		80		
LDR	Load Regulation[6]	V_{IN}=V_{OUT}+0.5V	LCON="H" 1mA≤I_{OUT}≤1A		10		mV
			LCON="L" 1mA≤I_{OUT}≤0.5A		5		
LNR	Line Regulation	V_{OUT}+1V≤V_{IN}≤5.5V （V_{IN}≥UVLO）			5	10	mV
I_Q	Quiescent Current	V_{OUT}=3.3V,I_{OUT}=0mA ,T_A=25℃			160		μA
I_{SHDN}	Standby Current	V_{EN}=0V			1	3	μA
I_{REV}	Reverse Current	V_{OUT}=V_{OSET}+1V， V_{EN}=0V， V_{IN}=0V			4.5	10	μA
I_{RUSH}	Start from EN Current Limit	CC mode	LCON="H"		500		mA
			LCON="L"		300		
PSRR	Power Supply Ripple Rejection	f=1kHz, Ripple=0.2Vp-p, V_{IN}=V_{SET}+1.0V, I_{OUT}=10mA,T_A=25℃			60		dB
e_{NO}	Output noise voltage （V_{OUT}=3V）	BW=10Hz to 100KHz， I_{OUT}=0mA,T_A=25 ℃			50		μV_{RMS}
		BW=10Hz to 100KHz， I_{OUT}=10mA,T_A=25 ℃			80		

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
$\frac{\Delta V_{OUT}}{\Delta T_A * V_{OUT}}$	Output Voltage Temperature Coefficient	-40 ºC≤T_A≤85 ºC		90		ppm/ºC
V_{ENH}	EN high voltage (enabled)	V_{IN}=5.5V, I_{OUT}=1mA, Full	1.2			V
V_{ENL}	EN low voltage (disabled)	V_{IN}=5.5V, I_{OUT}=1mA, Full			0.4	V
I_{LCON}	LCON Pull-down Current			0.2	1	μA
V_{LCONH}	LCON Input Voltage High		1.2			V
V_{LCONL}	LCON Input Voltage Low				0.4	V
T_{SD}	Thermal shutdown threshold			165		ºC
ΔT_{SD}	Thermal shutdown hysteresis			30		ºC
R_{DIS}	Output Discharge resistance	V_{IN}=4.0V, V_{EN}=0V, T_A=25℃		60		Ω

NOTE5: The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is $V_{OUT(NOM)}$*98%.

NOTE6: The Load regulation is measured using pulse techniques with duty cycle < 5%.

10. Typical Performance Characteristics

(T_A=-25 ºC, V_{IN}=V_{OUT}+1.0V, C_{IN} =4.7μF,C_{OUT}=1μF, unless otherwise noted)

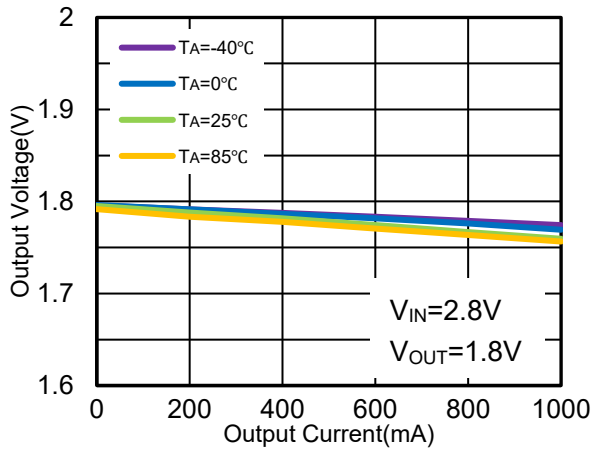


Figure 1. WR1006-18F18R
Load Regulation vs. Output Current

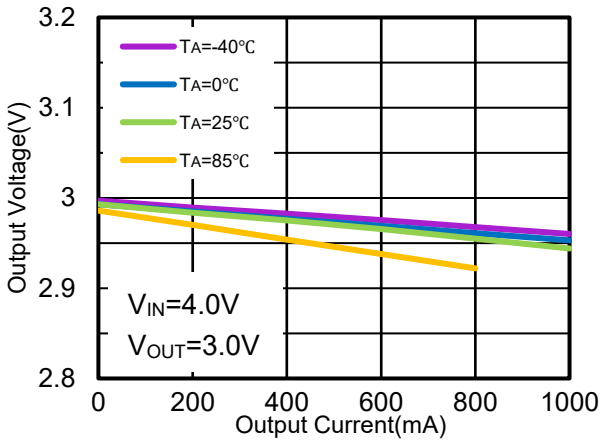


Figure 2. WR1006-30F18R
Load Regulation vs. Output Current

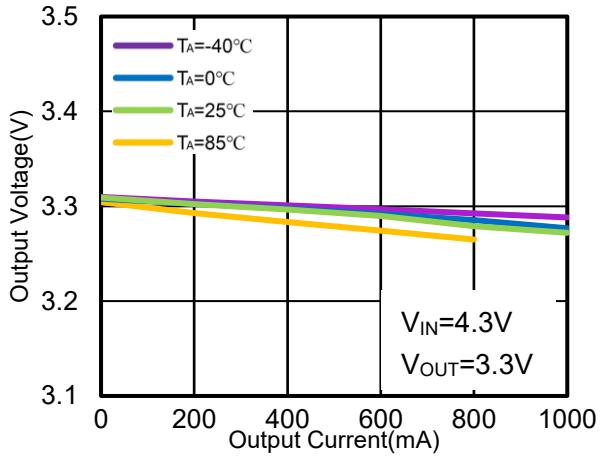


Figure 3. WR1006-33F18R
Load Regulation vs. Output Current

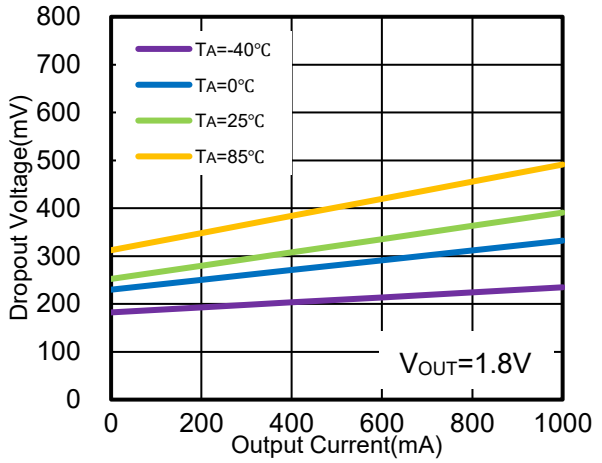


Figure 4. WR1006-18F18R
Dropout Voltage vs. Output Current

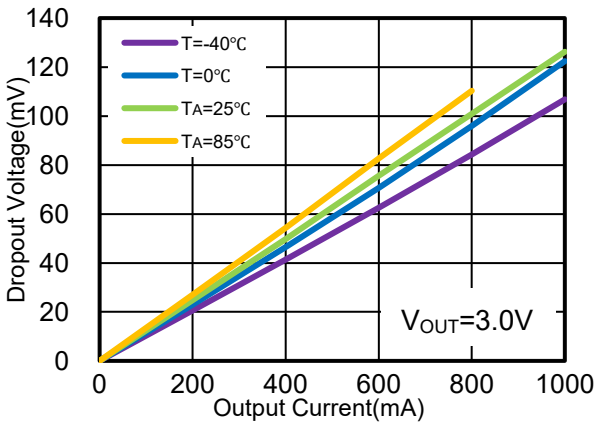


Figure 5. WR1006-30F18R
Dropout Voltage vs. Output Current

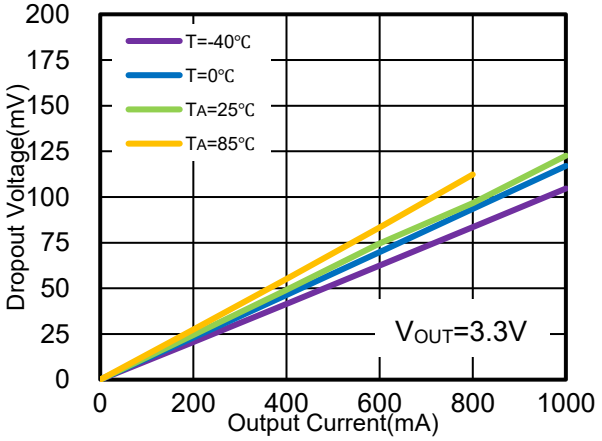


Figure 6. WR1006-33F18R
Dropout Voltage vs. Output Current

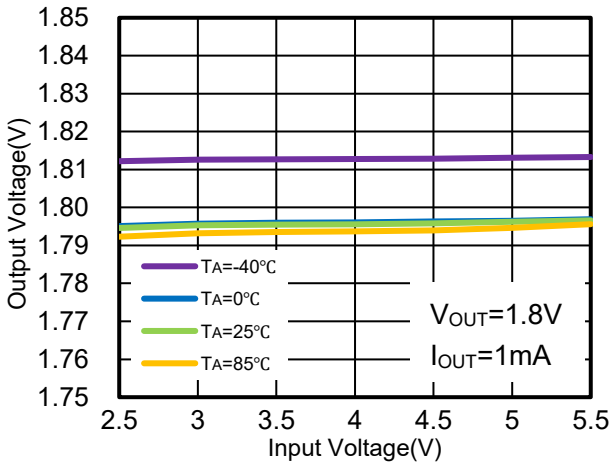


Figure 7. WR1006-18F18R
Regulation vs. V_{IN} (Line Regulation)

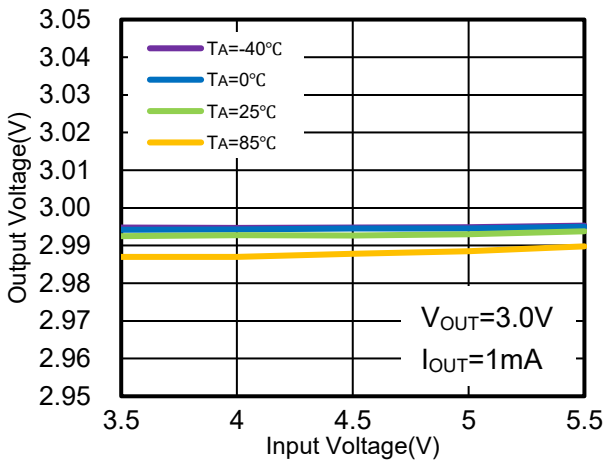


Figure 8. WR1006-30F18R
Regulation vs. V_{IN} (Line Regulation)

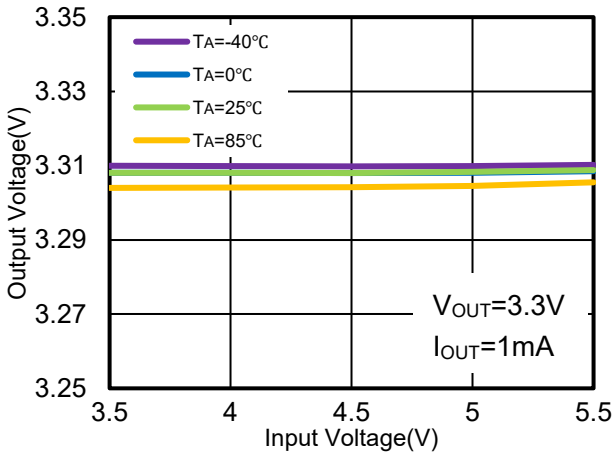


Figure 9. WR1006-33F18R
Regulation vs. V_{IN} (Line Regulation)

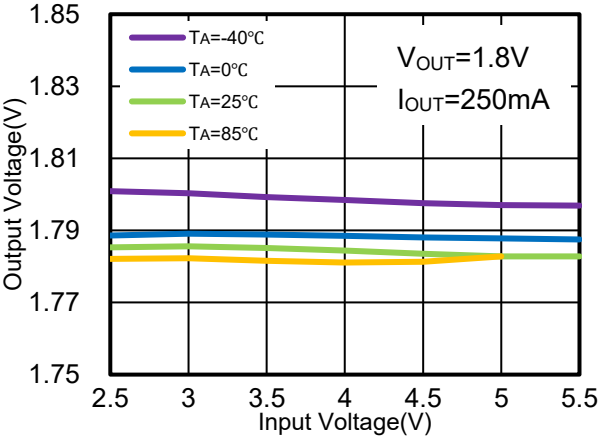


Figure 10. WR1006-18F18R
Regulation vs. V_{IN} (Line Regulation)

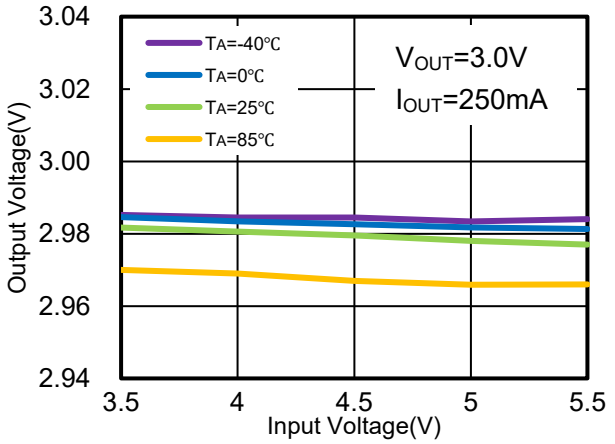


Figure 11. WR1006-30F18R
Regulation vs. V_{IN} (Line Regulation)

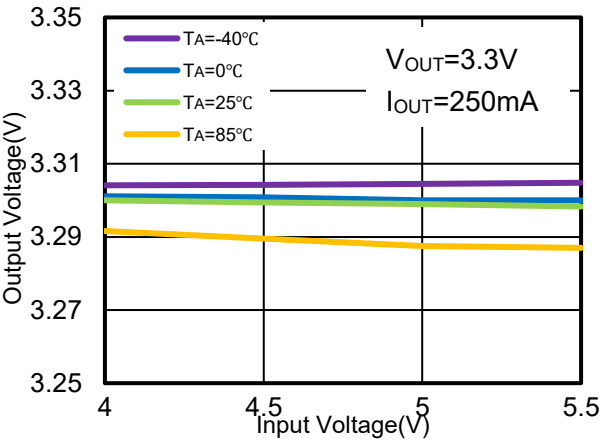


Figure 12. WR1006-33F18R
Regulation vs. V_{IN} (Line Regulation)

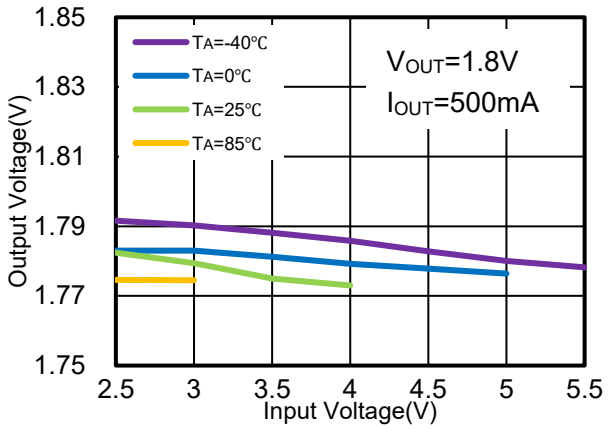


Figure 13. WR1006-18F18R
Regulation vs. V_{IN} (Line Regulation)

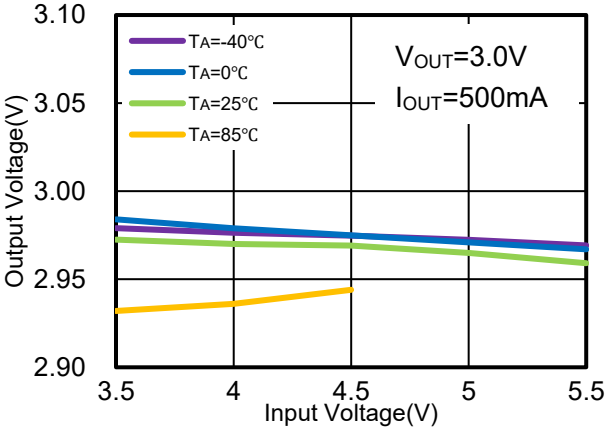


Figure 14. WR1006-30F18R
Regulation vs. V_{IN} (Line Regulation)

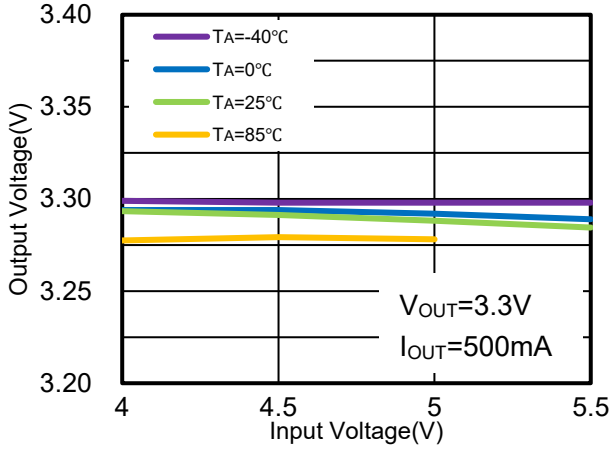


Figure 15. WR1006-33F18R
Regulation vs. V_{IN} (Line Regulation)

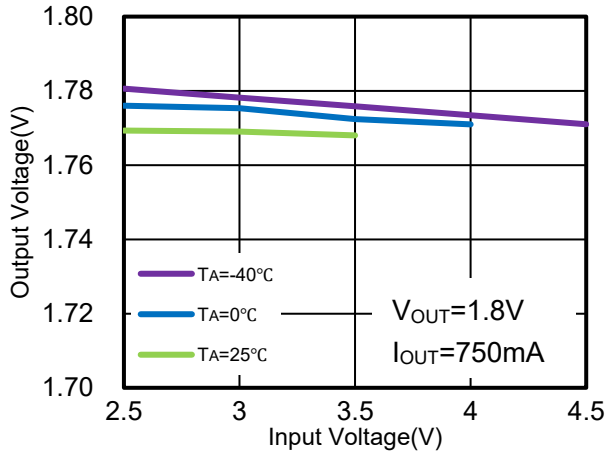


Figure 16. WR1006-18F18R
Regulation vs. V_{IN} (Line Regulation)

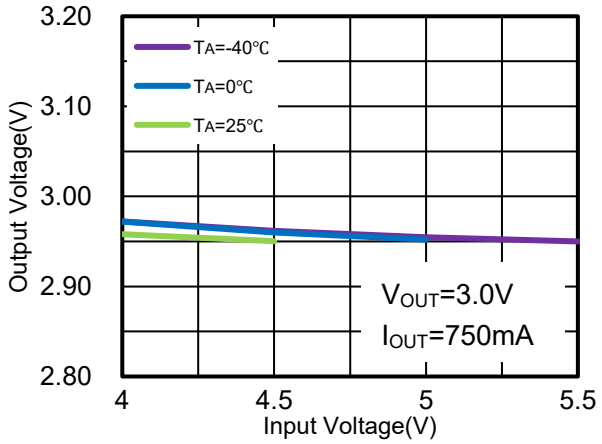


Figure 17. WR1006-30F18R
Regulation vs. V_{IN} (Line Regulation)

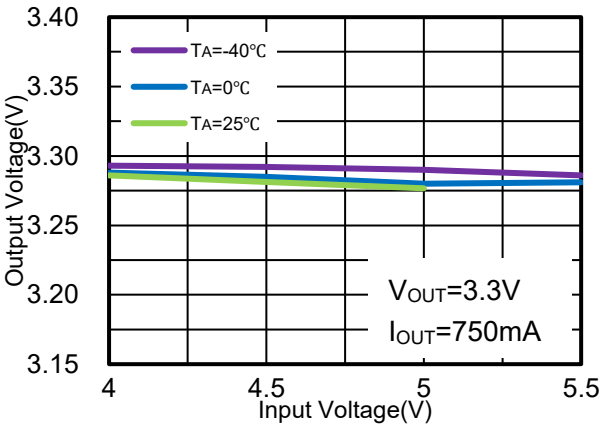


Figure 18. WR1006-33F18R
Regulation vs. V_{IN} (Line Regulation)

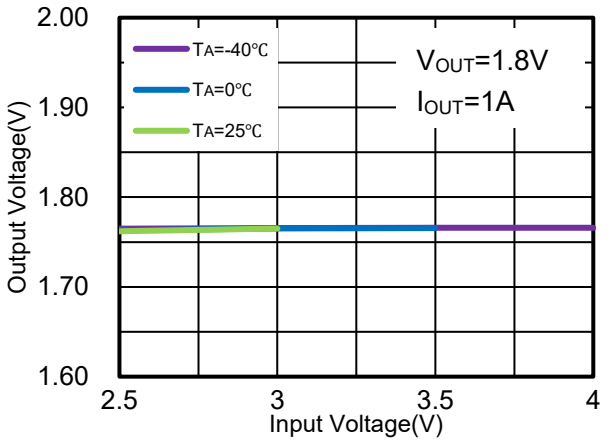


Figure 19. WR1006-18F18R
Regulation vs. V_{IN} (Line Regulation)

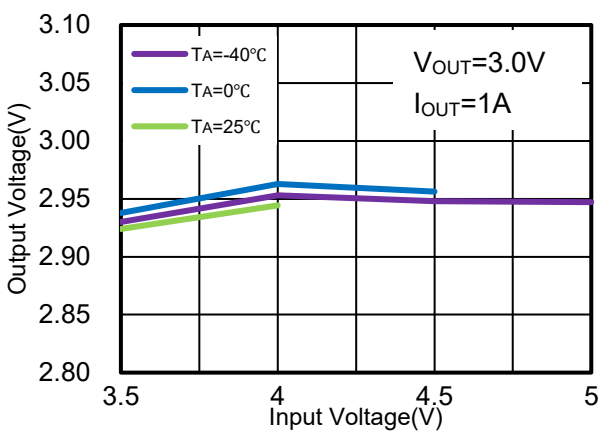


Figure 20. WR1006-30F18R
Regulation vs. V_{IN} (Line Regulation)

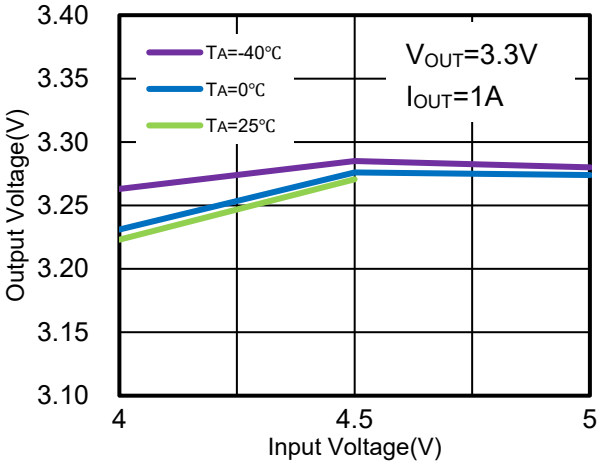


Figure 21. WR1006-33F18R
Regulation vs. V_{IN} (Line Regulation)

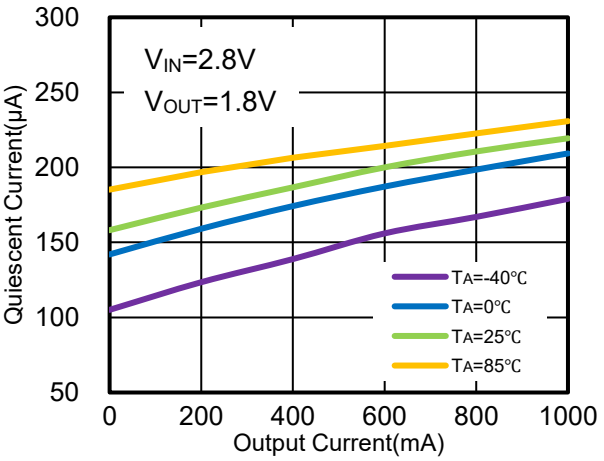


Figure 22. WR1006-18F18R
Ground Pin Current vs. I_{OUT}

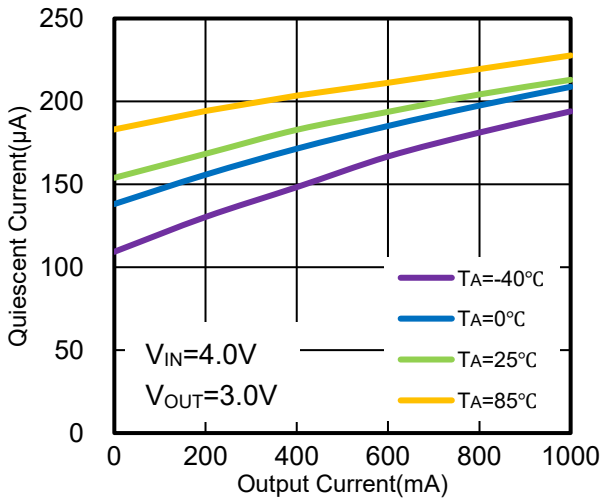


Figure 23. WR1006-30F18R
Ground Pin Current vs. I_{OUT}

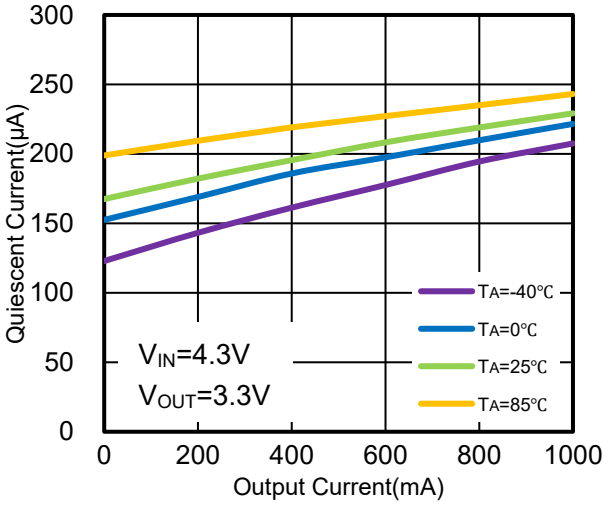


Figure 24. WR1006-33F18R
Ground Pin Current vs. I_{OUT}

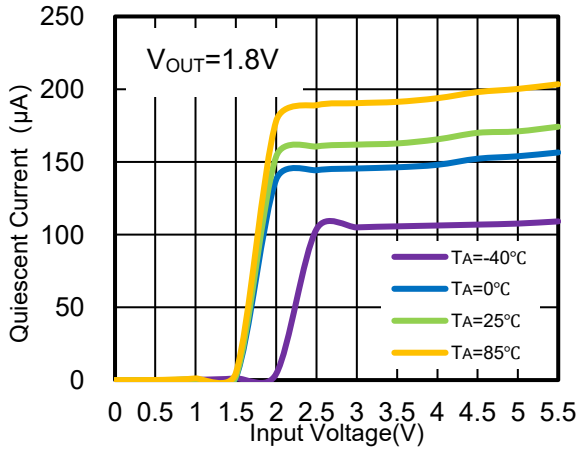


Figure 25. WR1006-18F18R
Quiescent Current vs. Input Voltage

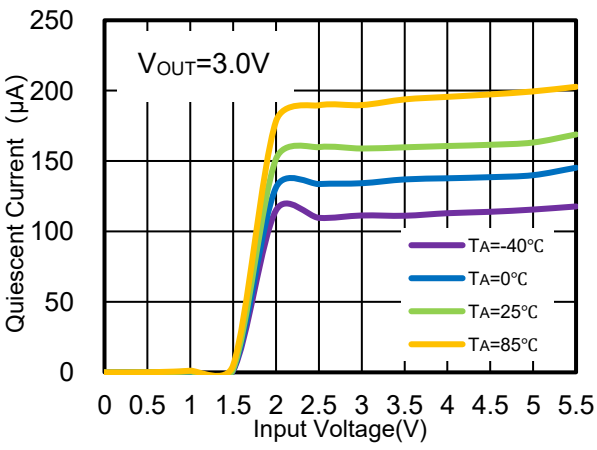


Figure 26. WR1006-30F18R
Quiescent Current vs. Input Voltage

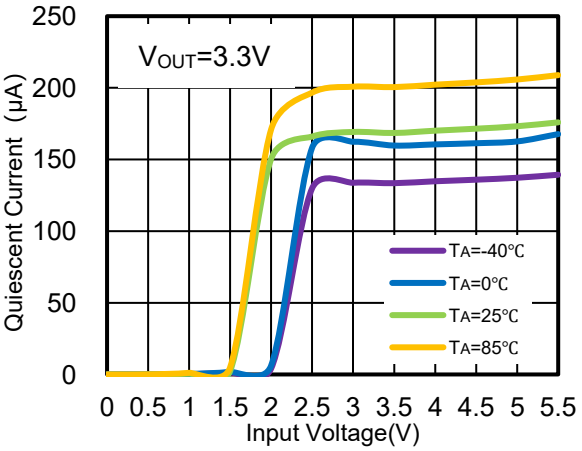


Figure 27. WR1006-33F18R
Quiescent Current vs. Input Voltage

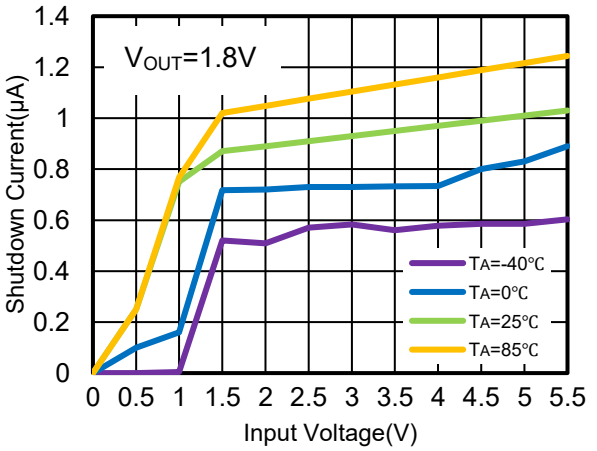


Figure 28. WR1006-18F18R
Shutdown Current vs. Input Voltage

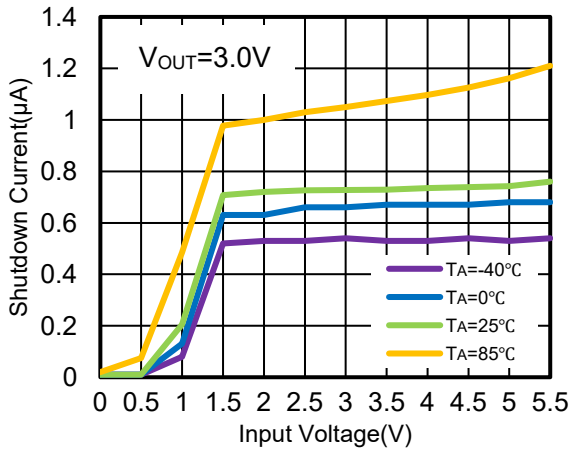


Figure 29. WR1006-30F18R
Shutdown Current vs. Input Voltage

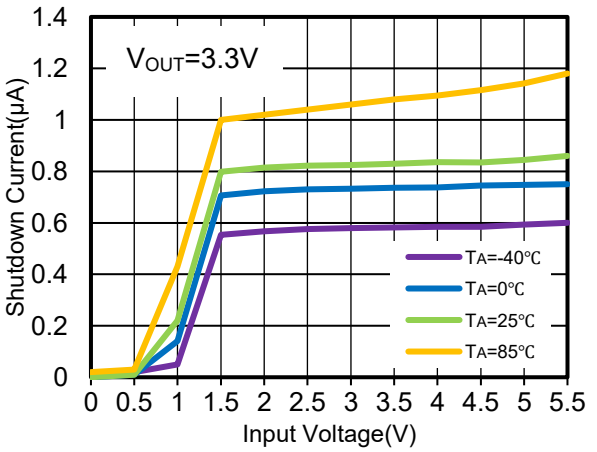


Figure 30. WR1006-33F18R
Shutdown Current vs. Input Voltage

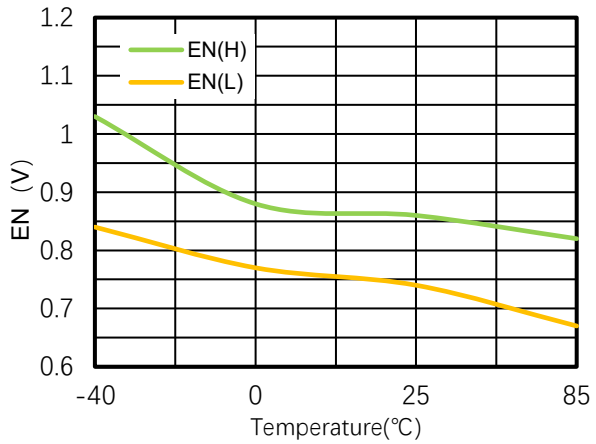


Figure 31. WR1006-18F18R
Enable Threshold vs. Ambient Temperature

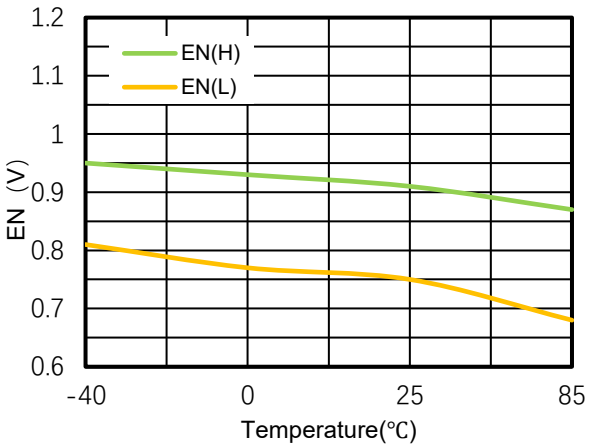


Figure 32. WR1006-30F18R
Enable Threshold vs. Ambient Temperature

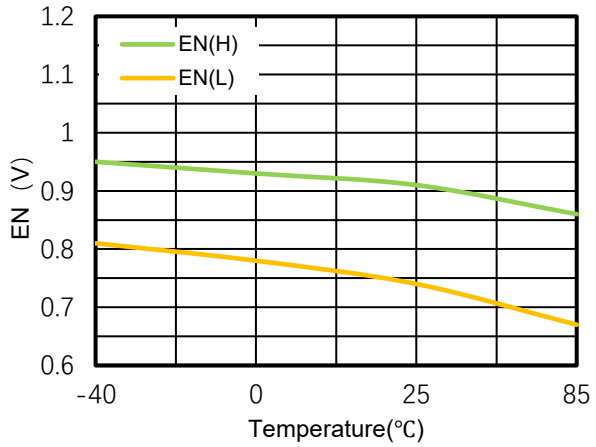


Figure 33. WR1006-33F18R
Enable Threshold vs. Ambient Temperature

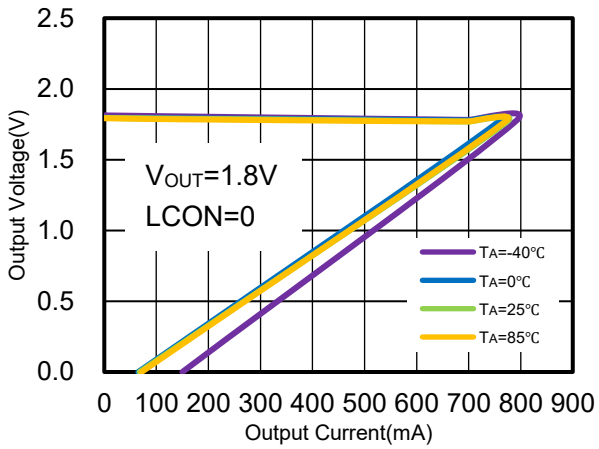


Figure 34. WR1006-18F18R
Foldback Current Limit vs. Output Current

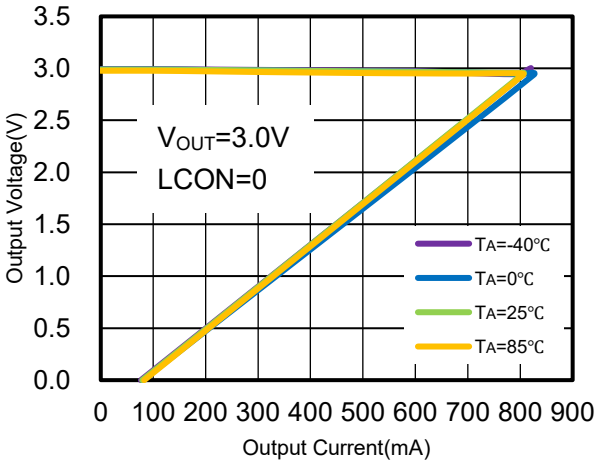


Figure 35. WR1006-30F18R
Foldback Current Limit vs. Output Current

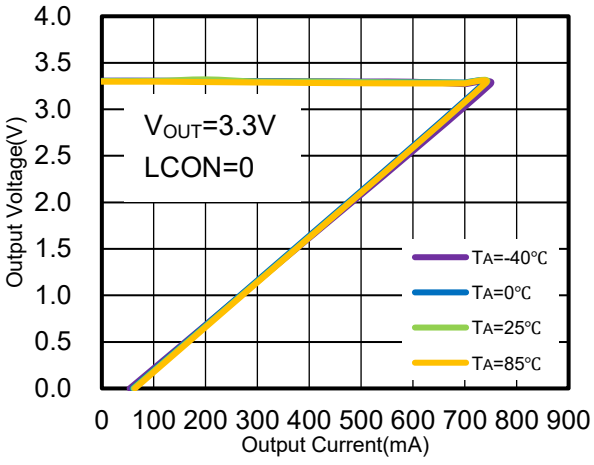


Figure 36. WR1006-33F18R
Foldback Current Limit vs. Output Current

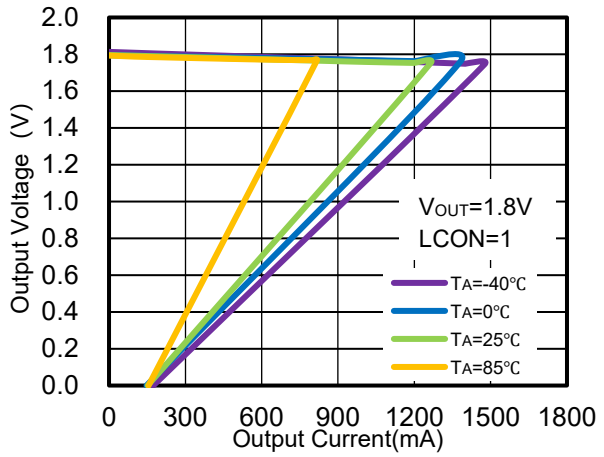


Figure 37. WR1006-18F18R
Foldback Current Limit vs. Output Current

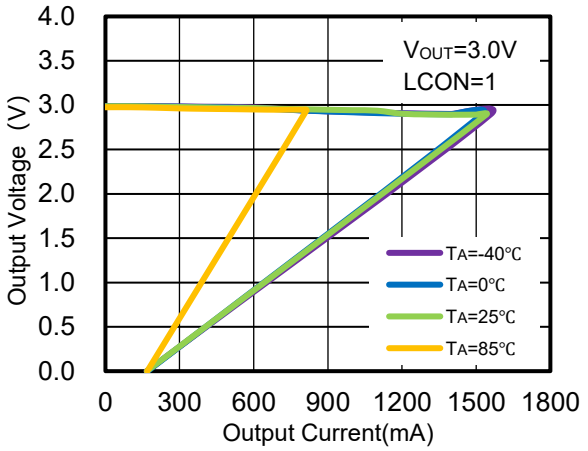


Figure 38. WR1006-30F18R
Foldback Current Limit vs. Output Current

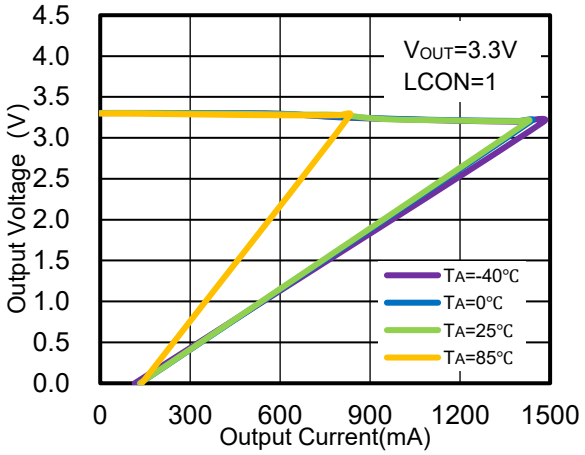


Figure 39. WR1006-33F18R
Foldback Current Limit vs. Output Current

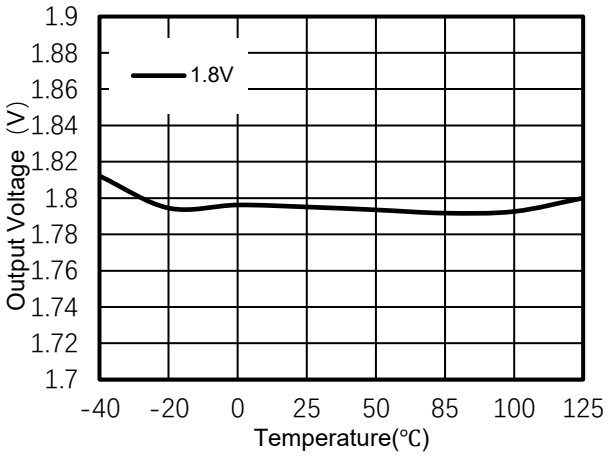


Figure 40. WR1006-18F18R
Output Voltage vs. Ambient Temperature

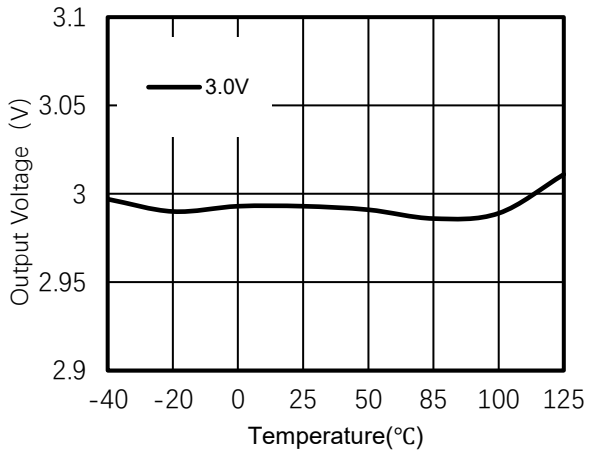


Figure 41. WR1006-30F18R
Output Voltage vs. Ambient Temperature

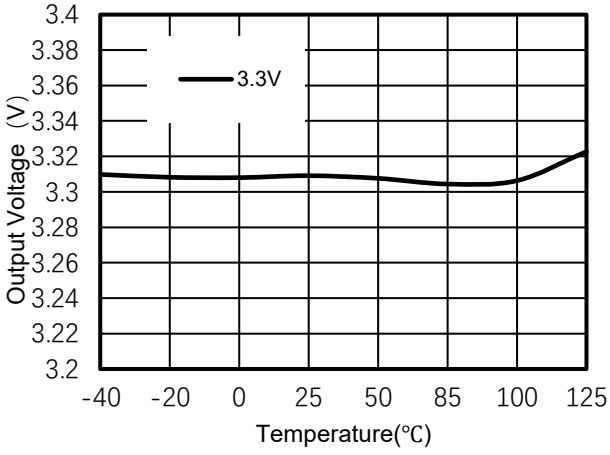


Figure 42. WR1006-33F18R
Output Voltage vs. Ambient Temperature

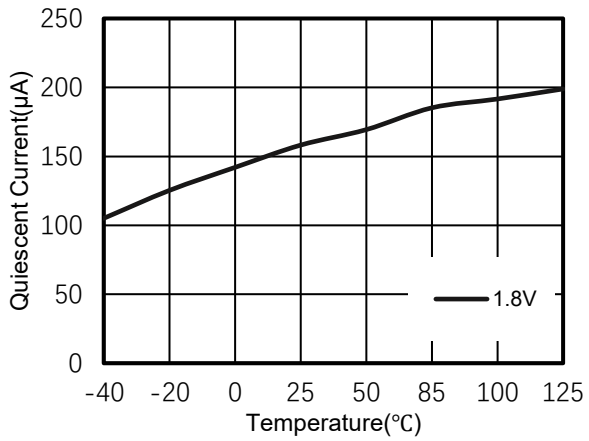


Figure 43. WR1006-18F18R
Quiescent Current vs. Ambient Temperature

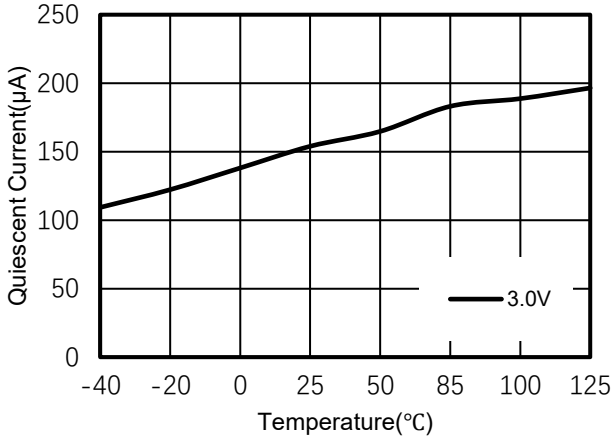


Figure 44. WR1006-30F18R
Quiescent Current vs. Ambient Temperature

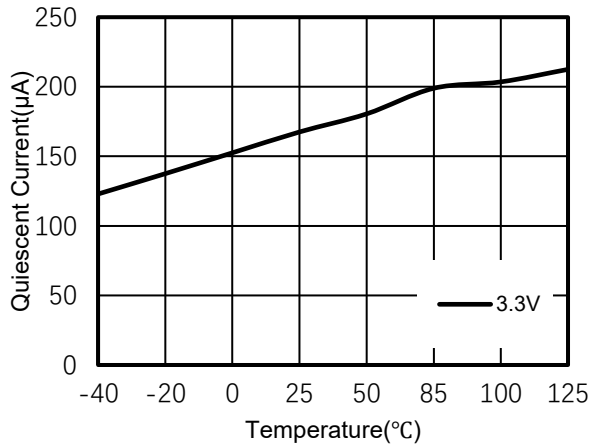


Figure 45. WR1006-33F18R
Quiescent Current vs. Ambient Temperature

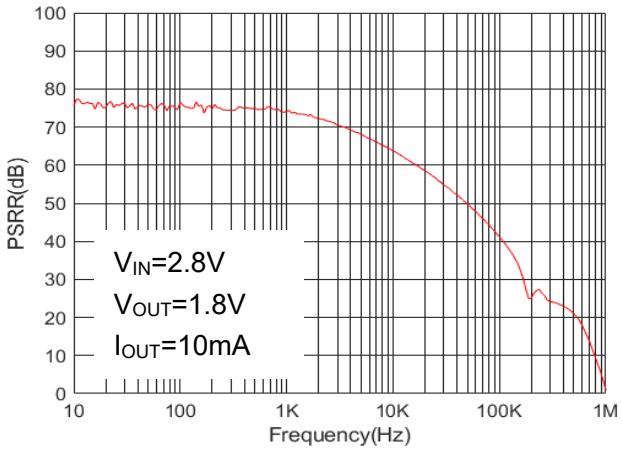


Figure 46. WR1006-18F18R
Power Supply Rejection Ratio vs. Frequency

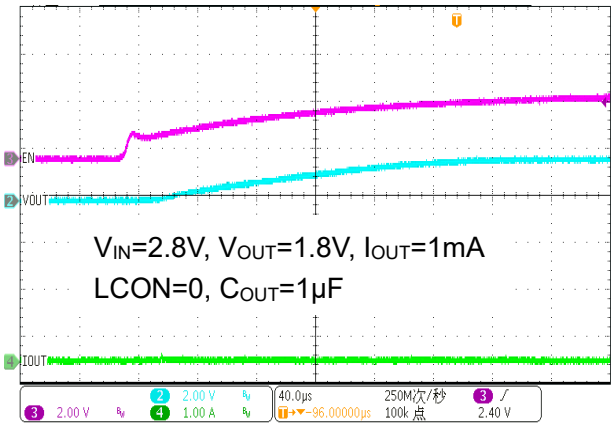


Figure 47. WR1006-18F18R
Soft Start from EN

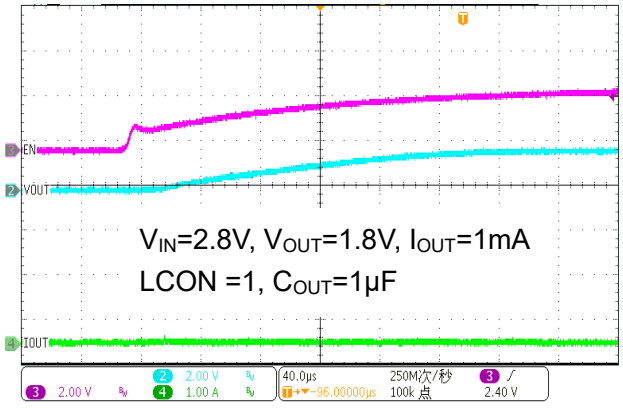


Figure 48. WR1006-18F18R
Soft Start from EN

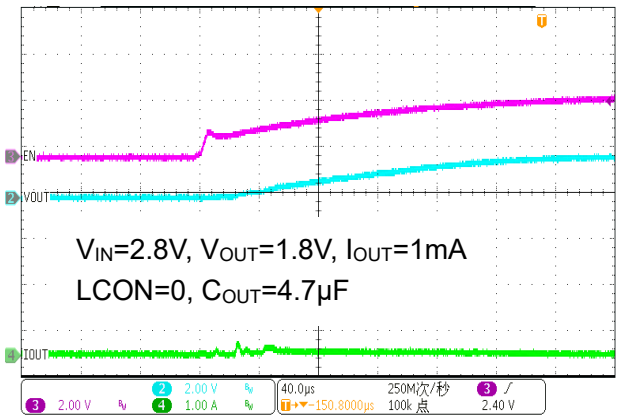


Figure 49. WR1006-18F18R
Soft Start from EN

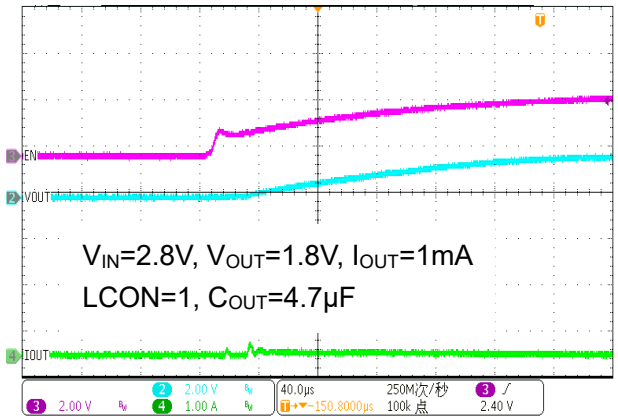


Figure 50. WR1006-18F18R
Soft Start from EN

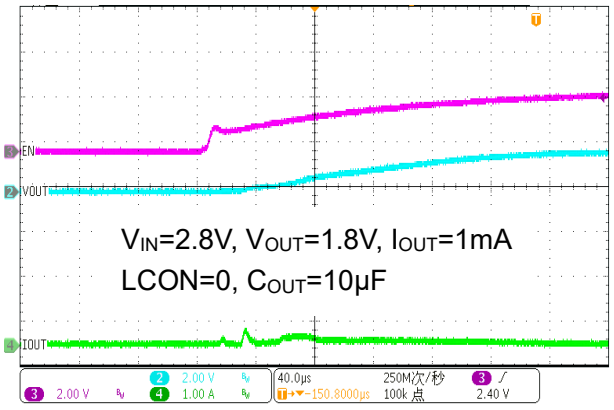


Figure 51. WR1006-18F18R
Soft Start from EN

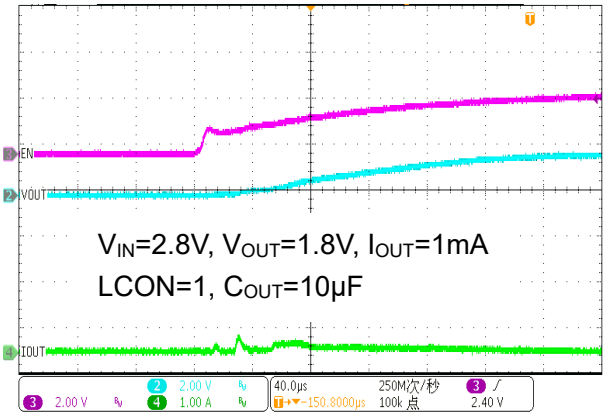


Figure 52. WR1006-18F18R
Soft Start from EN

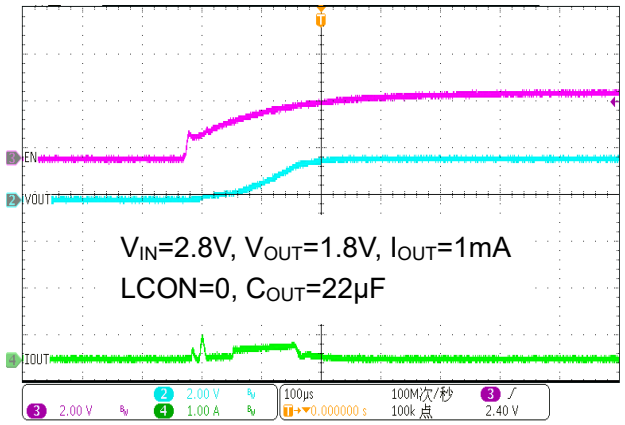


Figure 53. WR1006-18F18R
Soft Start from EN

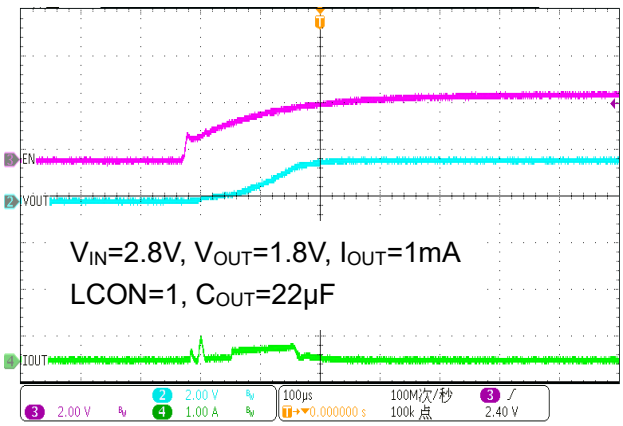


Figure 54. WR1006-18F18R
Soft Start from EN

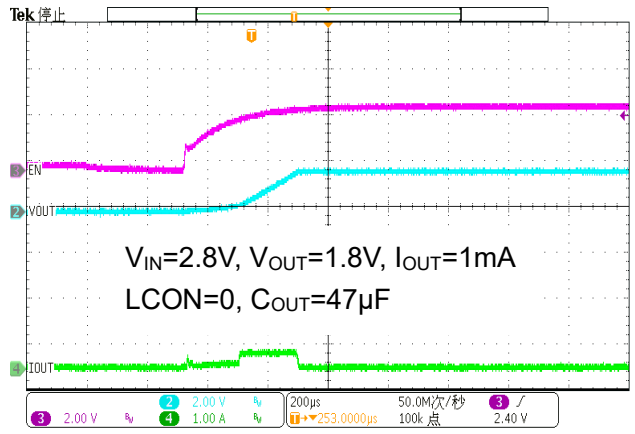


Figure 55. WR1006-18F18R
Soft Start from EN

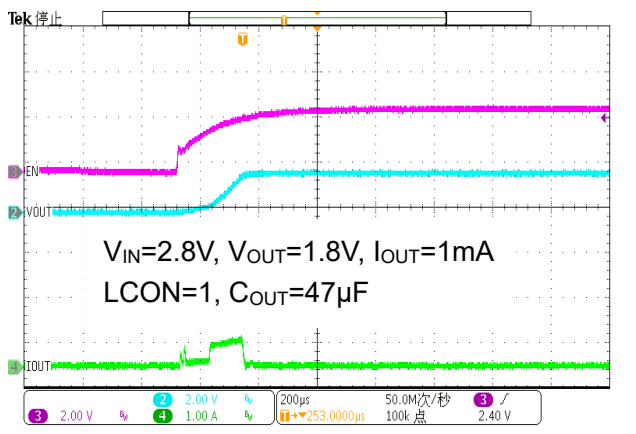


Figure 56. WR1006-18F18R
Soft Start from EN

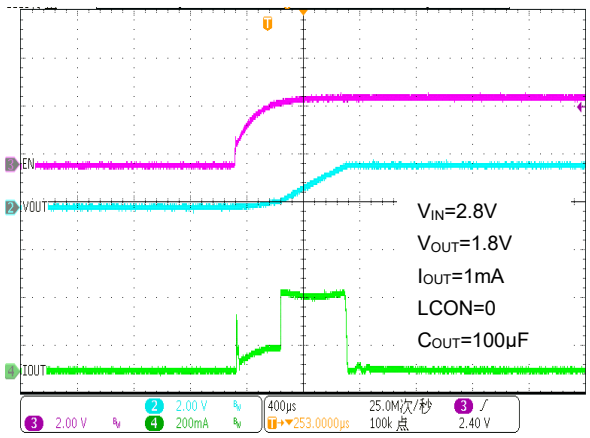


Figure 57. WR1006-18F18R
Soft Start from EN

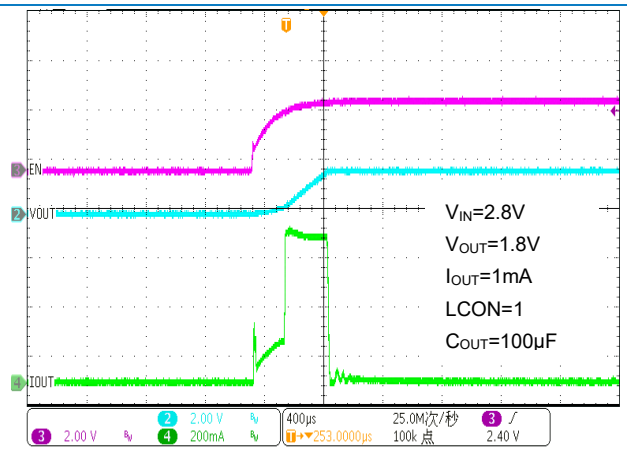


Figure 58. WR1006-18F18R
Soft Start from EN

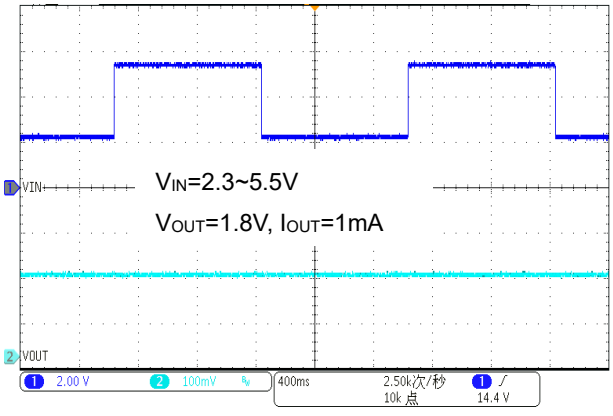


Figure 59. WR1006-18F18R
Line Transient

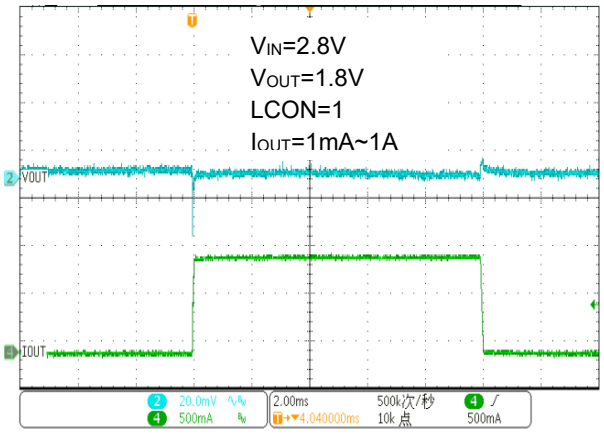


Figure 60. WR1006-18F18R
Load Transient

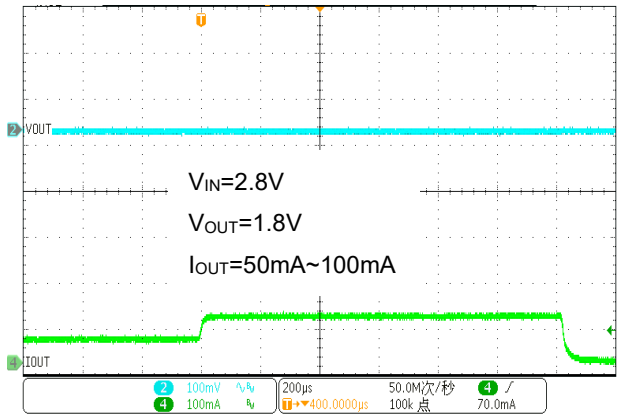


Figure 61. WR1006-18F18R
Load Transient

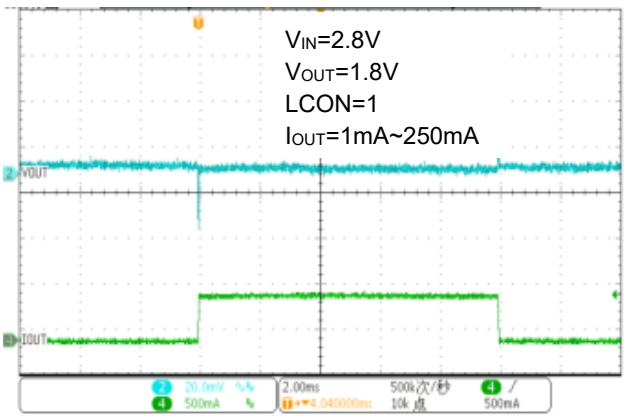


Figure 62. WR1006-18F18R
Load Transient

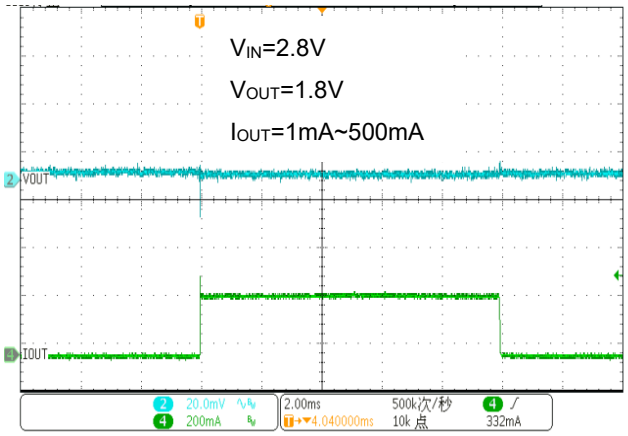


Figure 63. WR1006-18F18R
Load Transient

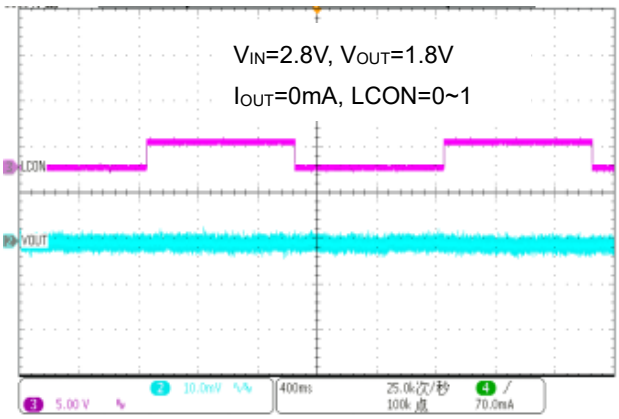


Figure 64. WR1006-18F18R
LCON Line Transient

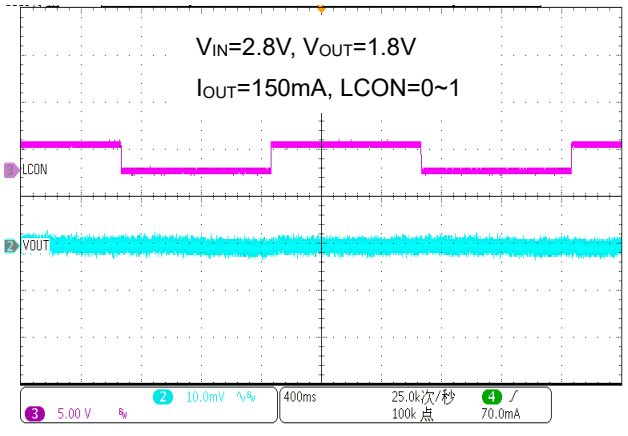


Figure 65. WR1006-18F18R
LCON Line Transient

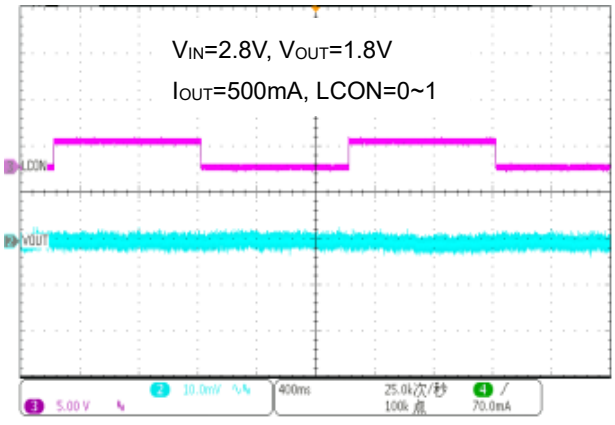


Figure 66. WR1006-18F18R
LCON Line Transient

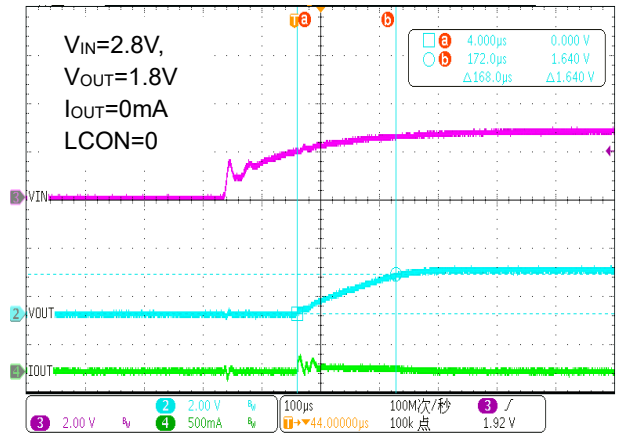


Figure 67. WR1006-18F18R
Power on

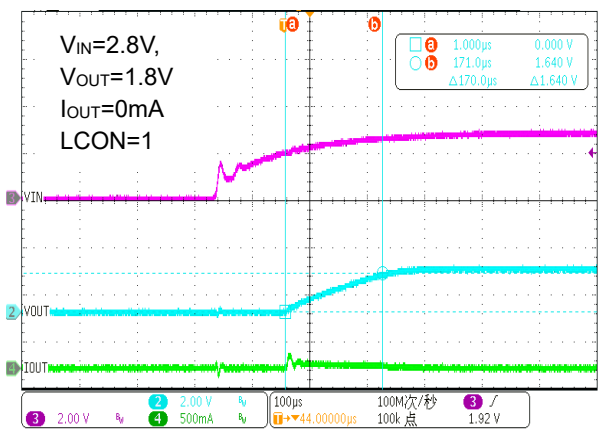


Figure 68. WR1006-18F18R
Power on

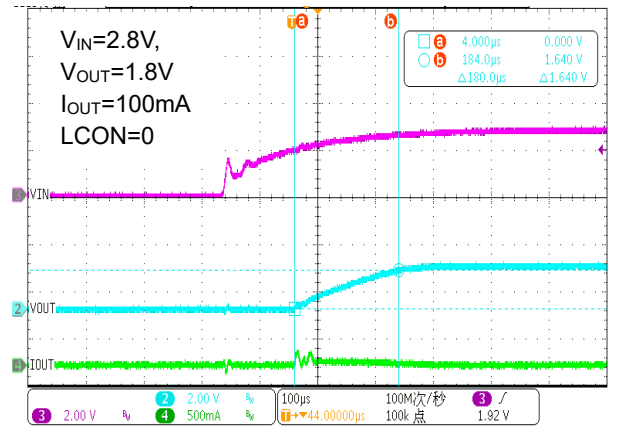


Figure 69. WR1006-18F18R
Power on

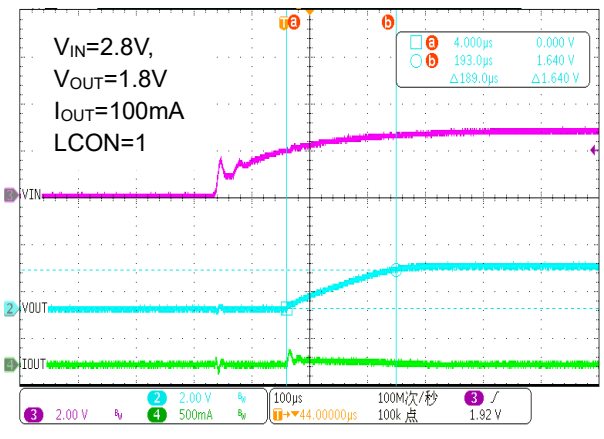


Figure 70. WR1006-18F18R
Power on

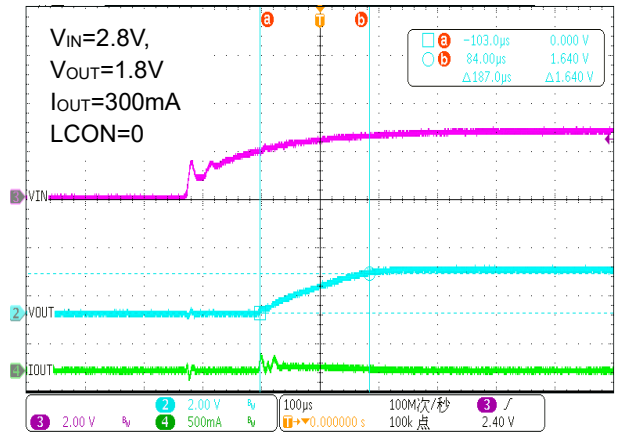


Figure 71. WR1006-18F18R
Power on

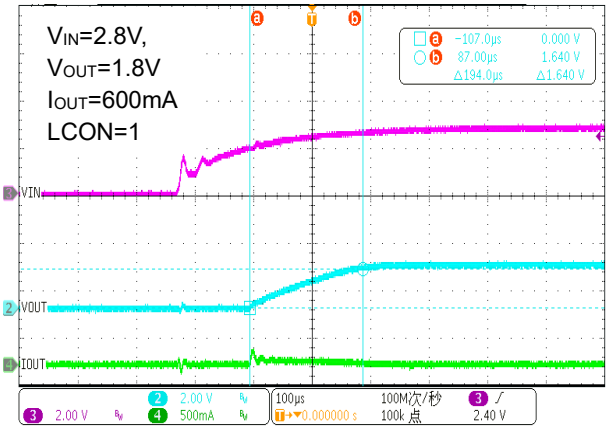


Figure 72. WR1006-18F18R
Power on

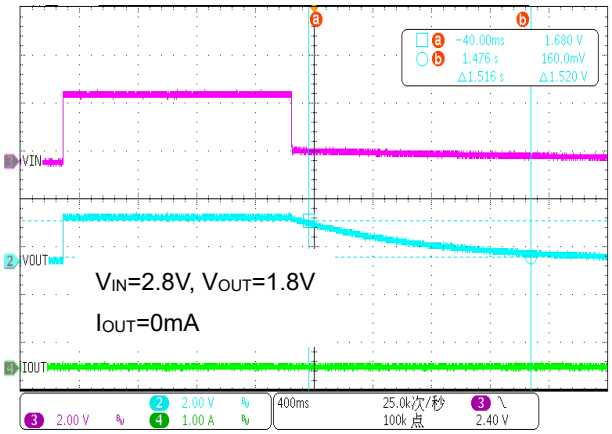


Figure 73. WR1006-18F18R
Shut Down

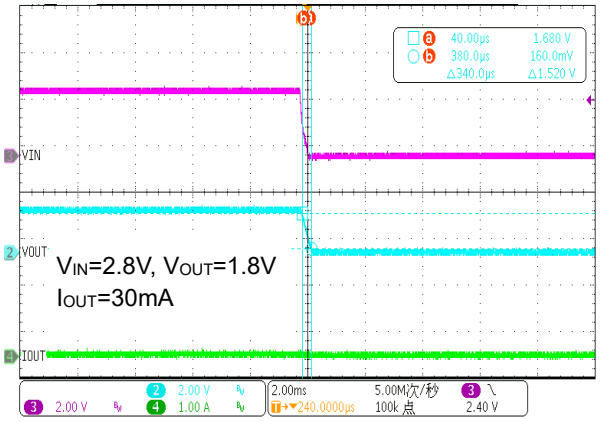


Figure 74. WR1006-18F18R
Shut Down

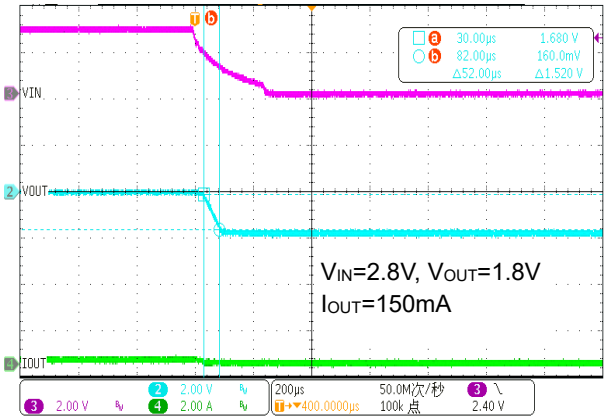


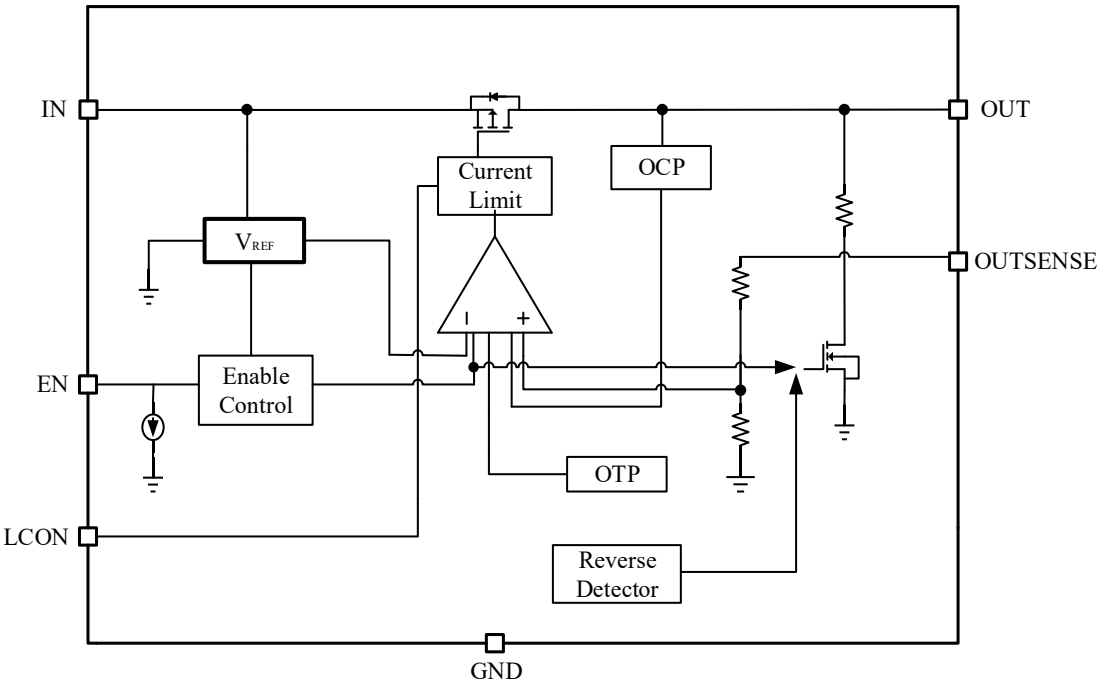
Figure 75. WR1006-18F18R
Shut Down

11. Function Description

11.1 Overview

The WR1006 series are CMOS-based low-dropout, low-power linear regulators, offering 500mA/1A with low dropout voltage, high ripple rejection, high output accuracy and low supply current. The WR1006 series consist of an accurate voltage-reference block, an error amplifier, a voltage-setting resistor net, a PMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit with short protection.

11.2 Block Diagram



11.3 Feature Description

11.3.1 Output Voltage Accuracy

The WR1006 has an output voltage accuracy of 2%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots.

11.3.2 Enable (EN)

When the input voltage of the enable pin is higher than the high enable voltage threshold, the device outputs normally. When the input voltage of the enable pin is lower than the low input voltage threshold of the EN pin, the device outputs shutdown. If you do not need to control the output voltage independently, connect the enable pin to the input of the device.

11.3.3 UVLO

When V_{IN} voltage is lower than UVLO，even when EN is high, the device will not start.

11.3.4 Dropout Voltage (V_{DO})

WR1006 has different Dropout voltages at high and low levels of LCON pins.Dropout voltage is defined as the V_{IN}-V_{OUT} at the rated maximum output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For CMOS regulators, the dropout voltage is determined by the $R_{DS\ (ON)}$ of the pass-FET.

The $R_{DS\ (ON)}$ is calculated as follows:.

$$R_{DS\ (ON)}=V_{DO}/I_{OUT}$$

11.3.5 Power Supply Rejection Ratio (PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$PSRR = 20lg\ (Ripple(in) / Ripple(out))$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR1006 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.6 Noise

LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics; external noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimising noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

The WR1006 has a low noise reference, high PSRR to ensure that output noise is reduced during normal operation.

11.3.7 Fold-back Current Limit (I_{LIM})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at IMAX, and the output voltage will be reduced to IMAXRLOAD.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current IMAX. The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to IFBRLOAD. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

WR1006 has different current limit values at high and low levels of LCON pins.More information on current limiting can be found in Electrical Characteristics Figure 34 to Figure 39.

11.3.8 Thermal Protection

The WR1006 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (TJ) of the energized crystal exceeds 165°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 135°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR1006's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR1006 into a thermal shutdown state will reduce the reliability of the device.

For reliable operation, limit the junction temperature to a maximum of 125°C. The thermal margin in a given layout is to be estimated. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition of the application.

11.3.9 Reverse Current Protection Circuit

The WR1006 include a Reverse Current Protection Circuit, which stop the reverse current from OUT pin to IN pin or GND pin when V_{OUT} becomes higher than V_{IN}.

Following figure shows the load characteristics of each mode. When giving the OUT pin a constant voltage and decreasing the V_{IN} voltage,the V_{IN} voltage will become lower than V_{OUT}-Vrev_det, the reverse current protection starts to function to stop the load current. By increasing the V_{IN} voltage higher than V_{OUT}-Vrev_rel, the protection mode will be released to let the load current to flow. When V_{IN} voltage is between V_{OUT} and Vrev_det, the parasitic diode between IN pin and OUT pin becomes forward direction. As a result, the current flows from OUT pin to IN pin, and the maximum of the current.

11.4 Device Functional Modes

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal	$5.5V>V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{ENH}$	$I_{OUT} < I_{LIM}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{ENH}$	$I_{OUT} < I_{LIM}$	$T_J < T_{SD}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{ENL}$	—	$T_J > T_{SD}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(NOM)}$ + V_{DO}) and is less than 5.5V.
2. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.
3. The output current is less than the current limit (I_{OUT} < I_{LIM}).
4. The device junction temperature is less than the thermal shutdown temperature (T_J < T_{SD}).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, but all other conditions are met for normal operation, the device operates in the dropout state and the output voltage tracks the input voltage. Because the transient performance of the device is significantly reduced through the device being in the triode state, the output current is no longer controlled. Line or load transients during power down can result in large output voltage deviations.

11.4.3 Disabled

The WR1006 can be turned off by forcing the enable pin low, typically with an enable voltage below 0.4V, at which point the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application and Implementation

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR1006 is a linear voltage regulator with an input voltage of 2.5 V to 5.5 V and an output voltage of 1.0 V to 3.3 V. The accuracy is 2% for output voltages. The maximum output current is 500 mA at LCON is low and 1A at LCON is high. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} – V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Start-Up

12.1.1.1 Inrush Current Limit

Constant slope circuit is included in the WR1006 to prevent the overshoot of the output voltage. If inrush current increases due to the large capacitance of C_{OUT}, the operation mode will be shift from Constant Slope (CS) mode to Constant Current (CC) mode. The CC mode maintains a constant inrush current. In the CC mode, ton varies with the size of C_{OUT} and the load current.

12.1.1.2 Automatic Discharge

The WR1006 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.2 Capacitor Recommendation

The WR1006 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN} and V_{OUT} pins to increase its stability. Multilayer ceramic capacitors are recommended. These capacitors also have limitations, and ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials have relatively good capacitance stability at different temperatures. WR1006 is designed to use ceramic capacitors of 4.7 μF or larger at the input and output. Place C_{IN} and C_{OUT} as close to the IN and OUT pins as possible to minimize trace inductance from the capacitor to the device.

Increasing the input capacitance can reduce the transient input drop during start-up and load current. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors can cause unwanted ringing at the OUT side, which requires well-designed short interconnects to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of several hundred milliohms in parallel with the ceramic input capacitor can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to a step change in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but at the same time the control loop bandwidth is reduced, which slows the response time.

Because, the LDO cannot consume charge, the control loop must close through the FET when the output load is removed or greatly reduced and wait for any excess charge to be depleted.

12.1.3 Power Dissipation (P_D)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

P_D can be calculated using the following equation:

$$\mathbf{P_D = (V_{IN} - V_{OUT}) \times I_{OUT}}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency.To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows

$$\mathbf{T_J = T_A + (R_{\theta JA} \times P_D)}$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Estimate the temperature of the junction

As recommended by JEDEC, the psi (Ψ) thermal metrics are used to estimate the junction temperature of the LDO in PCB board applications. These metrics are relative estimates of the junction temperature in actual applications. The thermal indicators ΨJT or ΨJB are given in the thermal information table and can be used according to the following equation.

Ψ_{JT}: TJ =TT + ΨJT x PD
Ψ_{JB}: TJ =TB + ΨJB x PD

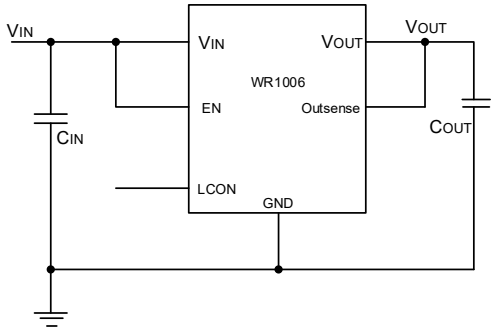
Notes.

1. P_D is the power dissipated.
2. T_T is the temperature at the top center of the device package.
3. T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package.

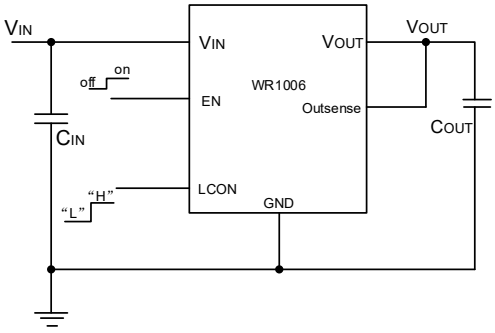
12.2 Typical Application

This section discusses the application of the WR1006 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic 1: V_{OUT} normally open, no control.



Circuit schematic 2: V_{OUT} control by external voltage to EN.



C_{IN} and C_{OUT} are to be selected with the recommended appropriate capacitance. 4.7μF ceramic capacitors are selected for C_{IN} ， 1μF ceramic capacitors are selected for C_{OUT} ， to help balance the charge needed to charge the output capacitor during startup, thus reducing the input voltage drop.

13. Power Supply Recommendations

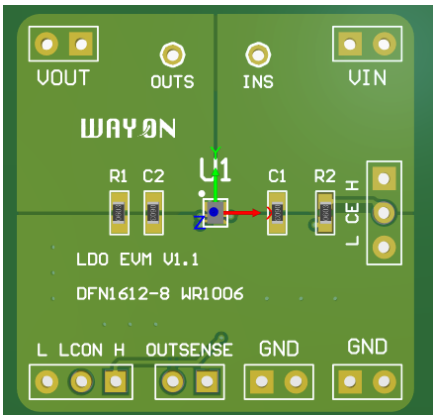
The WR1006 has a V_{IN} range of between 2.5 V and 5.5 V and an input capacitance of 4.7μF. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

14.1 Layout Example



15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

NAME	PACKAGE	EVALUATION MODULE
WR1006	DFN1612-8	WAYON LDO EVM V1.1-DFN1612-8

16. Naming Conventions

WR AA BB-CC DDD E

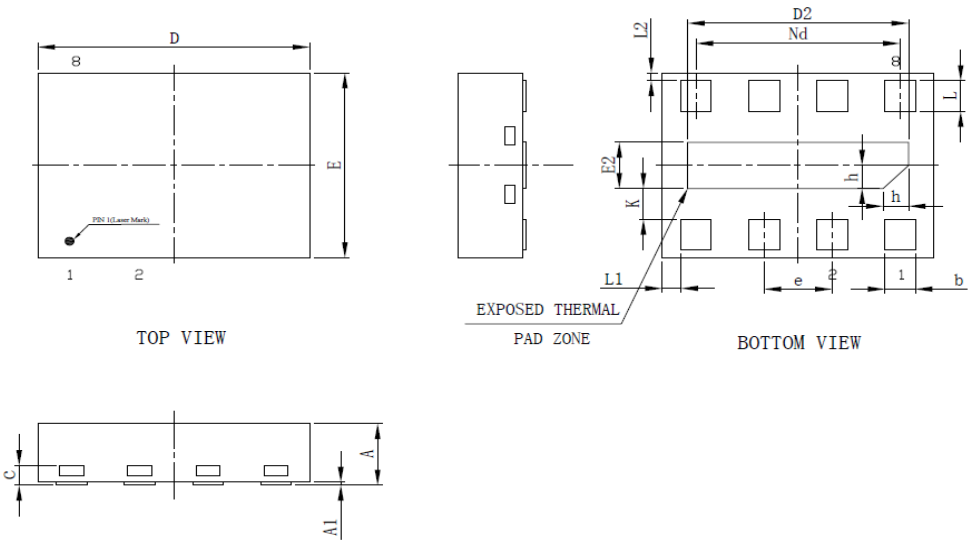
WR: WAYON Regulator;
AA: 10 –Output Current, 1A;
BB: Serial number;
CC: Output Voltage;
DDD: Package – F18: DFN1612-8
E: R-Reel & T-tube;

17. Electrostatic Discharge Warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

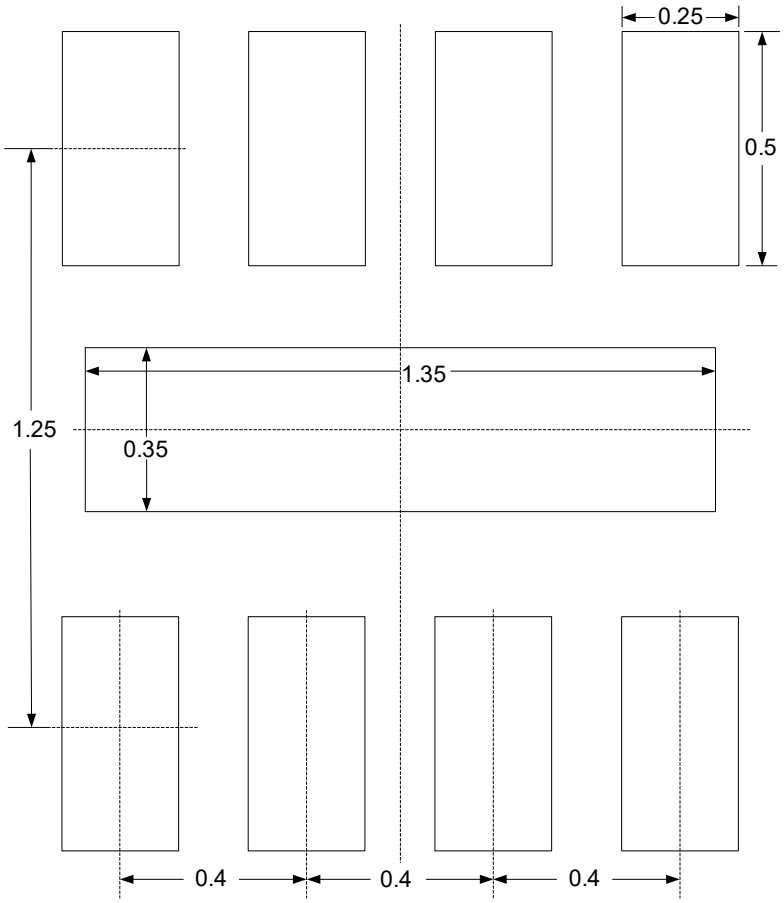
18. Package Information

DFN1612-8



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0	0.02	0.05
b	0.13	0.18	0.23
c		0.127REF	
D	1.55	1.60	1.65
D2	1.25	1.30	1.35
e		0.40BSC	
Nd		1.20BSC	
E	1.15	1.20	1.25
E2	0.25	0.30	0.35
L	0.15	0.20	0.25
L1	0.06	0.11	0.16
L2		0.05REF	
h	0.10	0.15	0.20
k	0.15	0.20	0.25

Suggested Pad Layout: DFN1612-8



NOTE: Dimensions in Millimeters

19. Ordering Information

PART NUMBER	OUTPUT VOLTAGE	PACKAGE	PACKING QUANTITY	MARKING*
WR1006-18F18R	1.8V	DFN1612-8	3k/Reel	006 18
WR1006-185F18R	1.85V	DFN1612-8	3k/Reel	006 185
WR1006-28F18R	2.8V	DFN1612-8	3k/Reel	006 28
WR1006-30F18R	3.0V	DFN1612-8	3k/Reel	006 30
WR1006-33F18R	3.3V	DFN1612-8	3k/Reel	006 33

Contact Information

No.1001, Shiwan(7) Road, Pudong District, Shanghai, P.R.China.201207
Tel: 86-21-50310888 Fax: 86-21-50757680 Email: market@way-on.com
WAYON website: http://www.way-on.com
For additional information, please contact your local Sales Representative.
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Product Specification Statement

1.The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.

2.The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. WAYON shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and WAYON assumes no responsibility for the application of the product.

3.WAYON strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, WAYON cannot guarantee that the information provided in the product specification is entirely accurate and error-free. WAYON shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications. WAYON reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with WAYON to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult WAYON in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.

4.Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.

5.The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. WAYON shall assume no responsibility for any consequences resulting from such usage.

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