WR0513

Ultra-Low Dropout, Input Voltage Range 5.5V, 500mA LDO

1. General Description

The WR0513 series are high performance positive voltage regulators with separated bias voltage (V_{BIAS}), offering output current up to 500mA with low dropout voltage and very low quiescent current for portable applications.

The feature of ultra-low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 0.8V and the output voltage is adjustable by an external resistive divider. In addition, the WR0513 series consist of an accurate voltage-reference block, Driver block, an error amplifier, a voltage-setting resistor net, a NMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit.

The WR0513 regulators are available in Green DFN1.2×1.2-6L, DFN1.2×1.2-4L packages.

2. Features

- Input Voltage Range: 0.8V to 5.5V
- Bias Voltage Range: 2.4V to 5.5V
- Output Voltage Range Fixed and Adjustable Versions: 0.6V to 3.3V(Fixed),
  0.8V to 3.6V (Adjustable)
- 1.5% Output Voltage Accuracy @25ºC
- Ultra-Low Dropout:
  180mV@V_{OUT}=3.3V, I_{OUT}=500 mA
- Bias Quiescent Current: 80μA (Typical)
- Bias Shut-down Current: 0.8μA (Typical)
- Enable Control
- Output Active Discharge Function(optional)
- Thermal Shutdown Protection: 170℃

3. Applications

- Battery Powered Systems
- Portable Electronic Device
- Digital Set Top Boxes

4. Typical Application Circuit

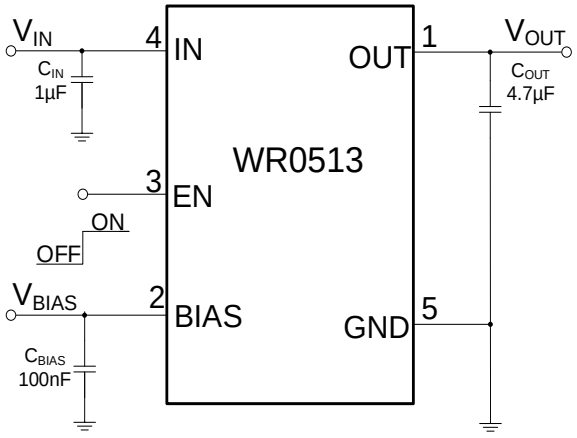
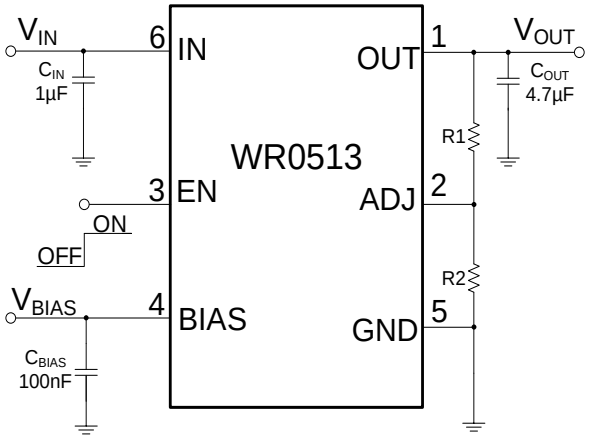


Figure 1. Fixed Voltage Regulator

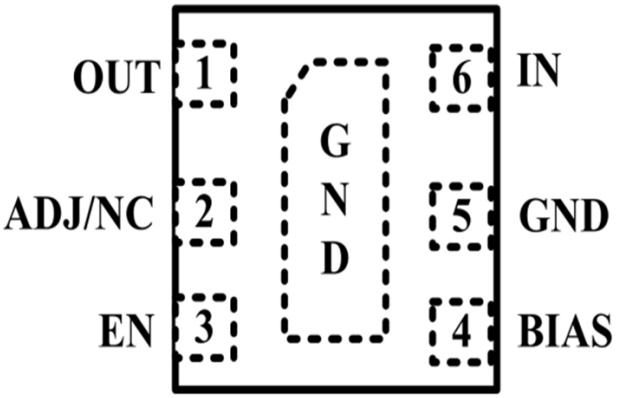


$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

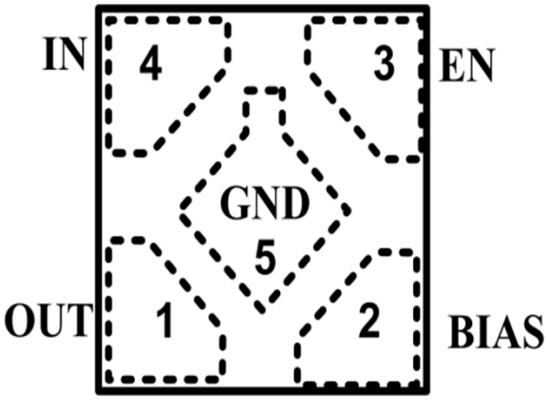
Figure 2. Adjustable Voltage Regulator

5. Pin Configuration

(Top View)



DFN1212-6L



DFN1212-4L

6. Pin Description

PIN NUMBER		PIN NAME	I/O	PIN FUNCTIONS
DFN1212-6L	DFN1212-4L			
1	1	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 4.7μF, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible.
2	-	ADJ/NC	I	ADJ: Adjustable output voltage feedback input. NC(FIX): This pin should be floating or connected to ground.
3	3	EN	I	Enable input. Active High. EN includes a small pull-down current source, nominally 0.5 μA.
4	2	BIAS	I	Supply voltage for the LDO control circuit. Mandatory to power up V_{BIAS} before V_{EN} and V_{IN} for the output soft start procedure works intended. The V_{BIAS} must be higher than 2.4V and ensure $V_{BIAS} \geq V_{OUT}$ + 1.6V for normal operation.
5	5	GND	-	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	4	IN	I	Input voltage supply. Bypass with a typical 1μF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.

7. Absolute Maximum Ratings[1]

SYMBOL	PARAMETER		RATING	UNIT
V_{IN}	Input Voltage range		-0.3 to 6.0	V
V_{EN}	EN Input voltage range		-0.3 to 6.0	
V_{OUT}	Output voltage range		-0.3 to 6.0	
I_{OUT}	Maximum output current		800	mA
P_D	Power Dissipation P_D @T_A = 25ºC	DFN1.2X1.2-6L	835	mW
		DFN1.2X1.2-4L	720	
$R_{\theta JA}$	Thermal resistance[2] [4] $R_{\theta JA}$	DFN1.2X1.2-6L	149.6	℃/W
		DFN1.2X1.2-4L	173.6	
$R_{\theta JB}$	Thermal resistance[2] [3] $R_{\theta JB}$	DFN1.2X1.2-6L	130.5	
		DFN1.2X1.2-4L	137	
$R_{\theta JC_T}$	Top Thermal resistance[2] [3] $R_{\theta JC}$	DFN1.2X1.2-6L	50.91	
		DFN1.2X1.2-4L	53.79	
$R_{\theta JC_B}$	Bottom Thermal resistance[2] [3] $R_{\theta JC}$	DFN1.2X1.2-6L	28.03	
		DFN1.2X1.2-4L	30.13	
T_J	Junction Temperature		150	℃
T_{SDR}	Lead Temperature Range		260	
T_{STG}	Storage Temperature Range		-65 to 150	
ESD	ESD Susceptibility	HBM	±4K	V

NOTE1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE2: Measured on 2cm x 2cm 2-layer FR4 PCB board, 2 oz copper, no via holes on GND copper.

NOTE3: Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

NOTE4: Power dissipation is calculate by $P_{D(MAX)} = (T_J - T_A) / R_{\theta JA}$.

8. Recommended Operating Conditions

SYMBOL	PARAMETER		RATING	UNIT
V_{IN}	Input voltage range		0.8 to 5.5	V
V_{BIAS}	V_{BIAS} Input voltage range		2.4 to 5.5	
V_{EN}	EN Input voltage range		0 to 5.5	
V_{OUT}	Nominal output voltage range	ADJ	0.8 to 3.6	
		FIX	0.6 to 3.3	
I_{OUT}	Output current range		0 to 500	mA
C_{IN}	Input capacitor		1.0	μF
C_{OUT}	Output capacitor		4.7	
C_{BIAS}	Bias capacitor		0.1	
T_A	Operating Temperature Range		-40 to 85	ºC

9. Electrical Characteristics

(V_{BIAS} = 2.4V or ($V_{OUT(NOM)}$ + 1.6V), whichever is greater, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = 1μF,C_{BIAS} = 0.1μF, C_{OUT} = 4.7μF, T_A=25ºC,unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
V_{IN}	Input Voltage			0.8		5.5	V
V_{BIAS}	Bias input Voltage			2.4		5.5	V
V_{OUT}	Output Voltage Accuracy	V_{OUT}=0.8V, no load		-0.5		0.5	%
		V_{OUT}+0.3V ≤ V_{IN} ≤ V_{OUT}+1V, 1mA ≤ I_{OUT} ≤ 500mA		-1.5		1.5	
V_{REF}	Reference Voltage (Adj devices only)			-	0.8	-	V
V_{UVLO}	Under Voltage Lock-Out	V_{BIAS} rising		-	1.6	-	V
		Hysteresis		-	0.2	-	
V_{DROP_IN}	V_{IN} Dropout Voltage[1]	I_{OUT}=150mA		-	37	75	mV
		I_{OUT}=500mA	V_{OUT}= 0.8V	-	120	250	
			V_{OUT}=1.05V	-	140	250	
			V_{OUT}= 1.2V	-	160	250	
			V_{OUT}= 3.3V	-	180	250	
V_{DROP_BIAS}	V_{BIAS} Dropout voltage[1]	V_{IN}= V_{BIAS}, I_{OUT}=500mA		-	1.2	1.6	V
ΔV_{LINE_IN}	V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.3V≤ V_{IN} ≤ 5V		-	0.01	-	%/V
ΔV_{LINE_BIAS}	V_{BIAS} Line Regulation	V_{BIAS} ≥ 2.4V and ($V_{OUT(NOM)}$ + 1.6V) ≤ V_{BIAS} ≤ 5.5V		-	0.01	-	%/V
ΔV_{LOAD}	Load Regulation	I_{OUT}=1mA to 500mA		-	5	-	mV
I_{LIM}	Output Current Limit	V_{OUT}= 90% $V_{OUT(NOM)}$		600	900	1200	mA
I_{OUT}	Output Current[2]	V_{OUT}= 98.5% $V_{OUT(NOM)}$		500	-	-	mA
I_{SHORT}	Short Current	V_{OUT}= 0 V		-	400	-	mA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
I_{ADJ}	ADJ Pin Operation Current (ADJ devices only)		-	0.1	0.5	μA
I_{BIAS}	Bias Pin Operating Current		-	80	110	μA
$I_{BIAS(DIS)}$	Bias Pin Shutdown Current	$V_{EN} \leq 0.4V$	-	0.8	1.5	μA
$I_{IN(DIS)}$	V_{IN} Pin Shutdown Current	$V_{EN} \leq 0.4V$	-	0.5	1	μA
V_{ENH}	Enable Threshold Voltage	Logic _ High	0.9	-	-	V
V_{ENL}		Logic _ Low	-	-	0.5	V
I_{EN}	EN Pull Down Current	V_{EN}=5.5V, V_{BIAS}=5.5V	-	0.5	-	μA
t_{ON}	Turn-On Time	From assertion of V_{EN} to V_{OUT} =90% $V_{OUT(NOM)}$), $V_{OUT(NOM)}$ = 1V	-	150	-	μs
PSRR_V_{IN}	Power Supply Rejection Ratio	$V_{IN} \geq V_{OUT}$ + 0.5V, V_{IN} to V_{OUT} , f=1kHz, I_{OUT} = 100mA,	-	70	-	dB
PSRR_V_{BIAS}		$V_{IN} \geq V_{OUT}$ + 0.5V, V_{BIAS} to V_{OUT}, f = 1kHz, I_{OUT} = 100mA,	-	65	-	dB
e_{NO_FIXED}	Output Noise Voltage (Fixed Volt.)	V_{IN}=V_{OUT}+0.5V, $V_{OUT(NOM)}$=1V, f=10Hz to 100kHz	-	40	-	μV_{RMS}
e_{NO_ADJ}	Output Noise Voltage (Ad Volt.)	V_{IN} =V_{OUT}+0.5V, f=10Hz to 100kHz	-	50* V_{OUT}	-	μV_{RMS}
T_{SD}	Thermal Shutdown Threshold	Temperature increasing	-	170	-	°C
		Temperature decreasing	-	145	-	°C
R_{DISCHG}	Output Discharge Pull-Down	V_{EN}<0.4V, V_{OUT}=0.5V	-	150	-	Ω

NOTE1: The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is $V_{OUT(NOM)}$*97%.

NOTE2: Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN}< V_{OUT} + V_{DROP}.

NOTE3: The Load regulation is measured by pulse test.

10. Typical Performance Characteristics

(V_{BIAS} = 2.4V or ($V_{OUT(NOM)}$ + 1.6V), whichever is greater, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{BIAS} = 0.1μF, C_{OUT} =4.7μF, T_A = -40℃ to +85℃, unless otherwise noted.)

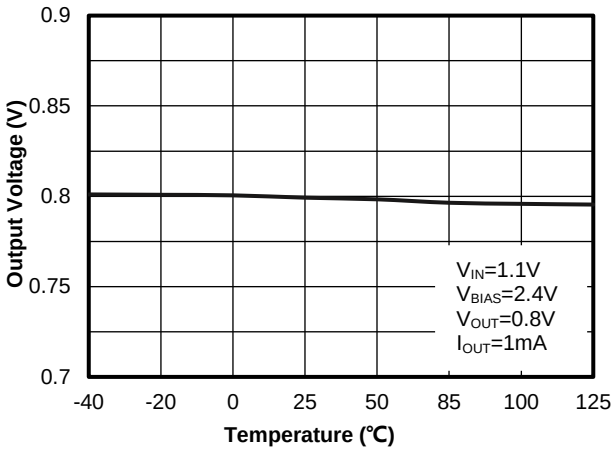


Figure 1. WR0513-ADF16R (0.8V)
Output Voltage vs. Ambient Temperature

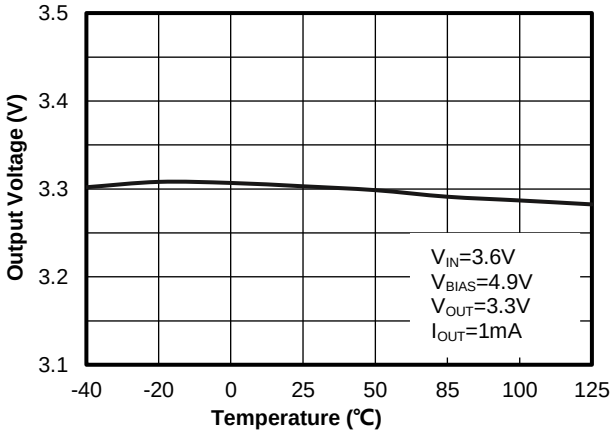


Figure 2. WR0513-ADF16R (3.3V)
Output Voltage vs. Ambient Temperature

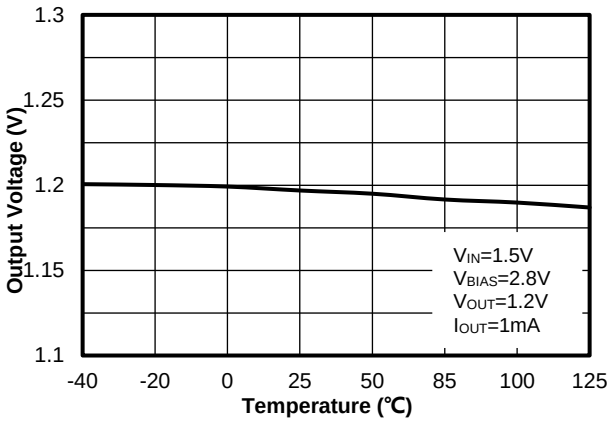


Figure 3. WR0513-12F14R
Output Voltage vs. Ambient Temperature

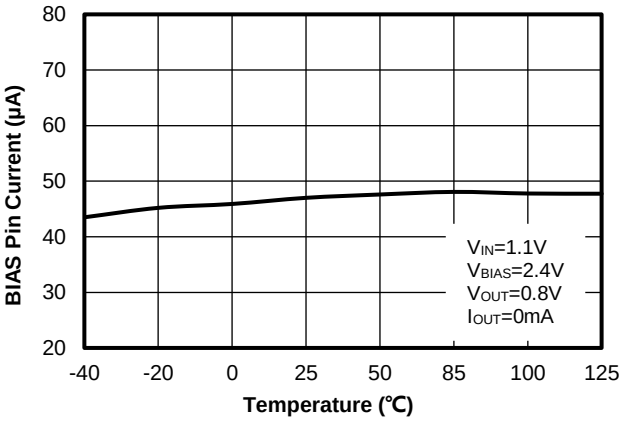


Figure 4. WR0513-ADF16R (0.8V)
Bias Pin Current vs. Ambient Temperature

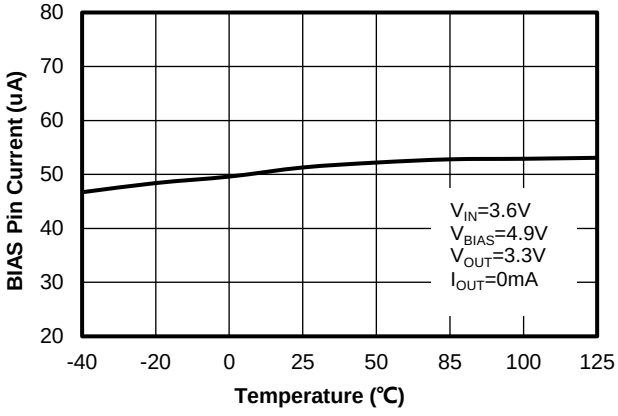


Figure 5. WR0513-ADF16R (3.3V)
Bias Pin Current vs. Ambient Temperature

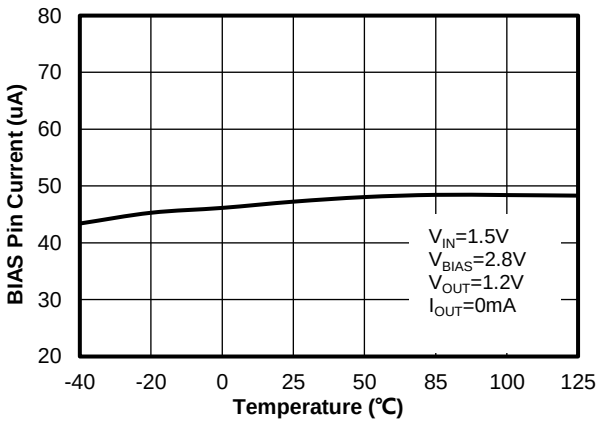


Figure 6. WR0513-12F14R
Bias Pin Current vs. Ambient Temperature

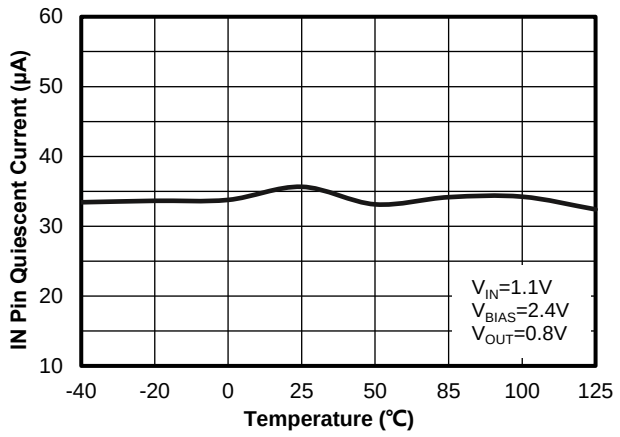


Figure 7. WR0513-ADF16R (0.8V)

IN Pin Current vs. Ambient Temperature

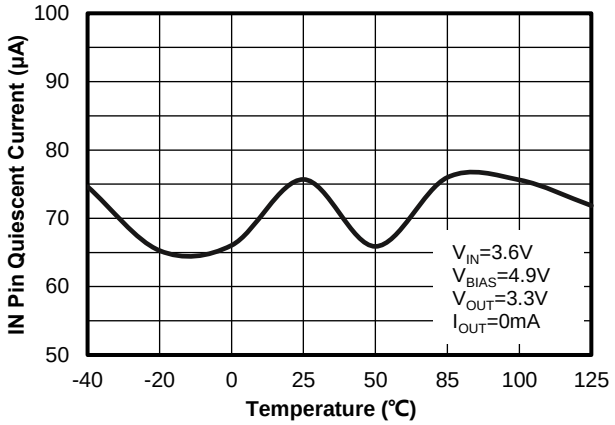


Figure 8. WR0513-ADF16R (3.3V)

IN Pin Current vs. Ambient Temperature

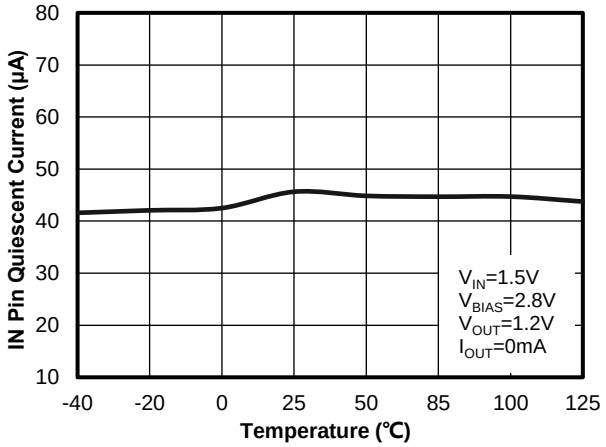


Figure 9. WR0513-12F14R

IN Pin Current vs. Ambient Temperature

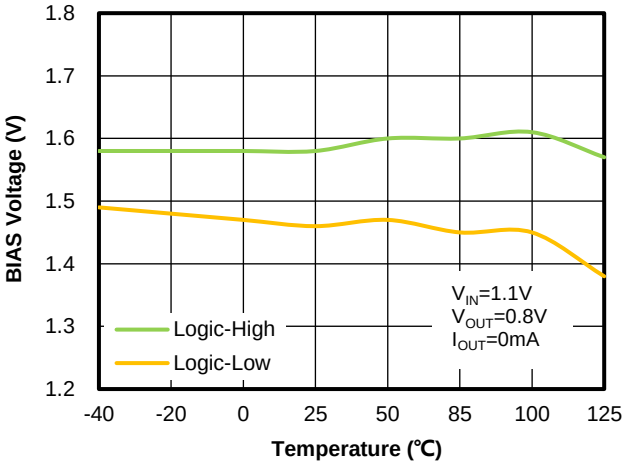


Figure 10. WR0513-ADF16R (0.8V)

BIAS Voltage UVLO vs. Ambient Temperature

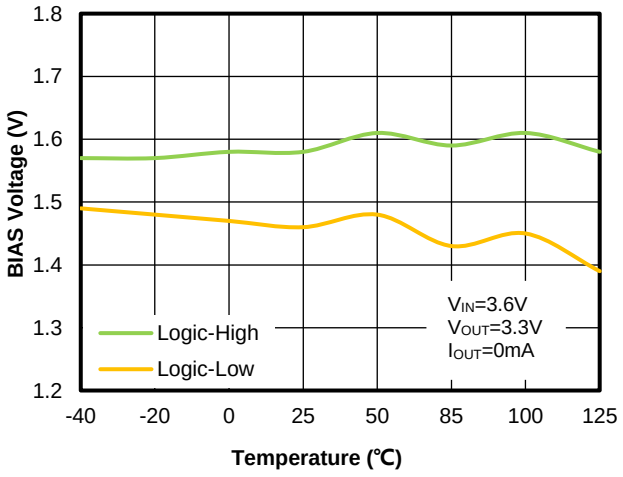


Figure 11. WR0513-ADF16R (3.3V)

BIAS Voltage UVLO vs. Ambient Temperature

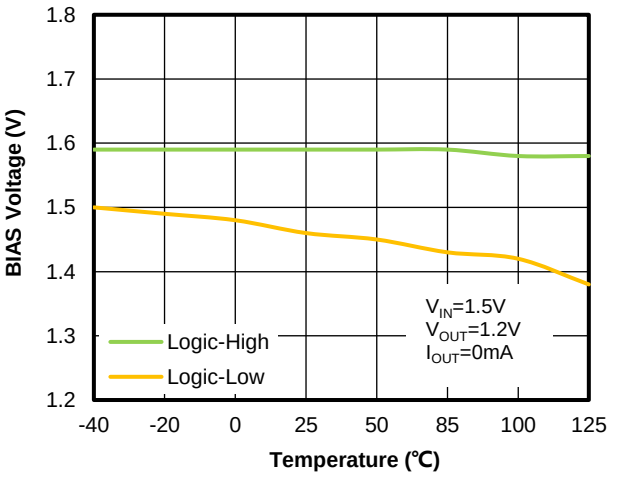


Figure 12. WR0513-12F14R

BIAS Voltage UVLO vs. Ambient Temperature

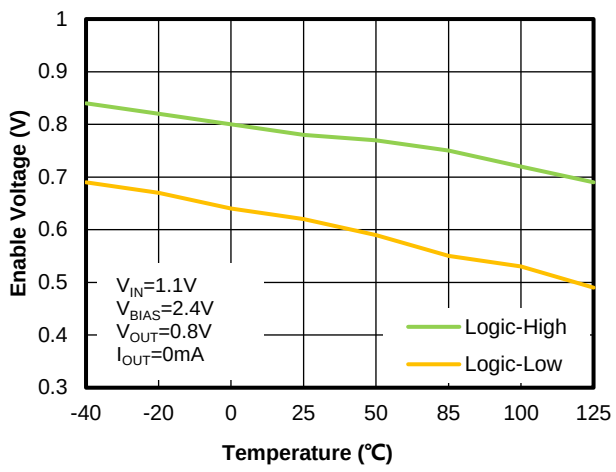


Figure 13. WR0513-ADF16R (0.8V)

Enable Voltage Threshold vs. Ambient Temperature

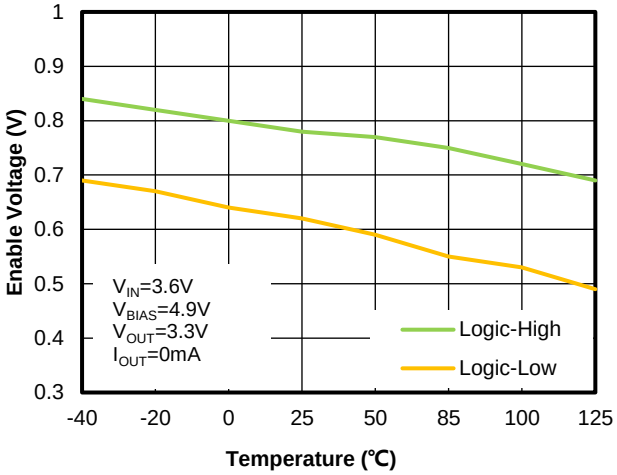


Figure 14. WR0513-ADF16R (3.3V)

Enable Voltage Threshold vs. Ambient Temperature

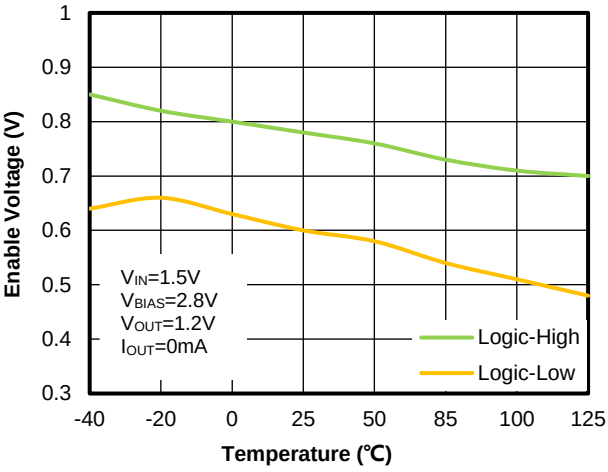


Figure 15. WR0513-12F14R

Enable Voltage Threshold vs. Ambient Temperature

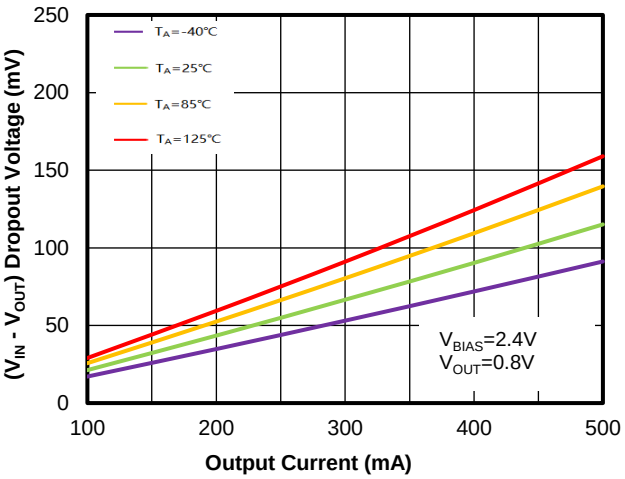


Figure 16. WR0513-ADF16R (0.8V)

IN Dropout Voltage vs. Ambient Temperature

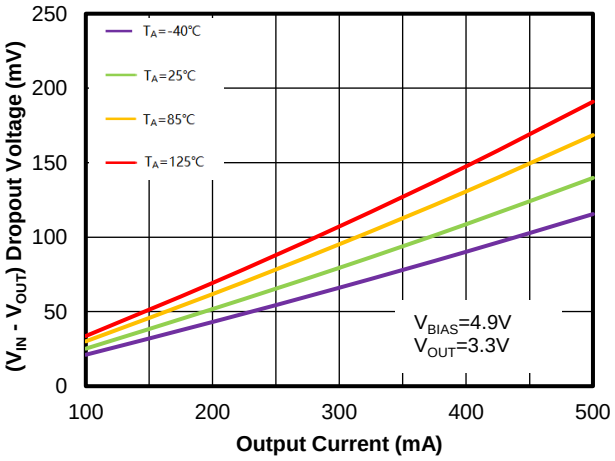


Figure 17. WR0513-ADF16R (3.3V)

IN Dropout Voltage vs. Ambient Temperature

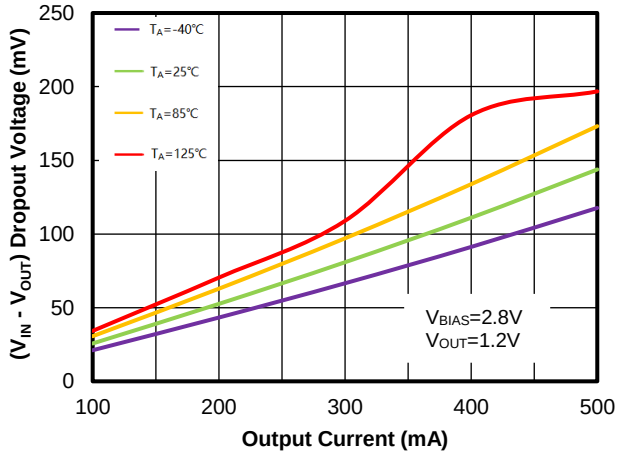


Figure 18. WR0513-12F14R

IN Dropout Voltage vs. Ambient Temperature

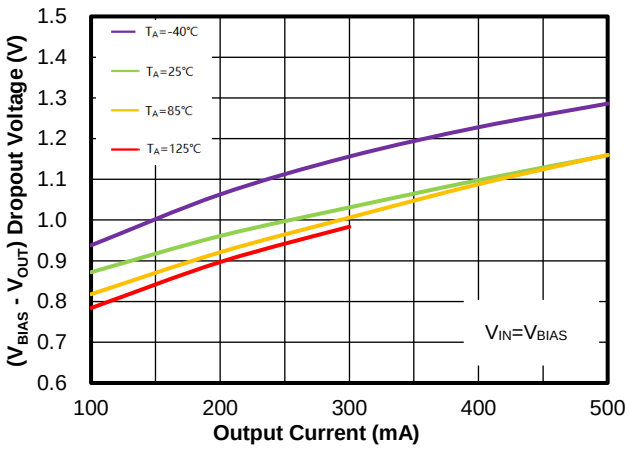


Figure 19. WR0513-ADF16R (0.8V)

BIAS Dropout Voltage vs. Ambient Temperature

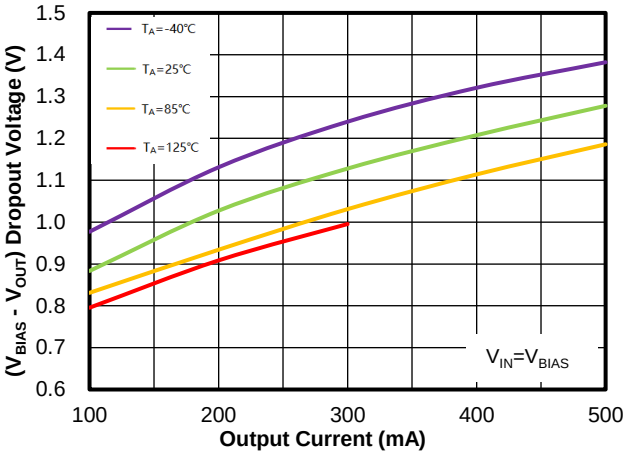


Figure 20. WR0513-ADF16R (3.3V)

BIAS Dropout Voltage vs. Ambient Temperature

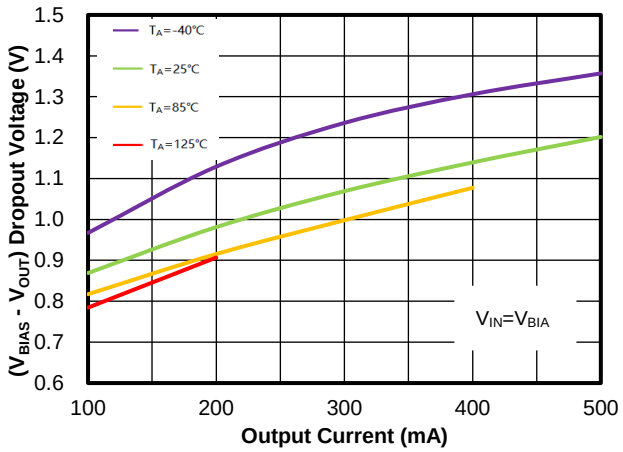


Figure 21. WR0513-12F14R

BIAS Dropout Voltage vs. Ambient Temperature

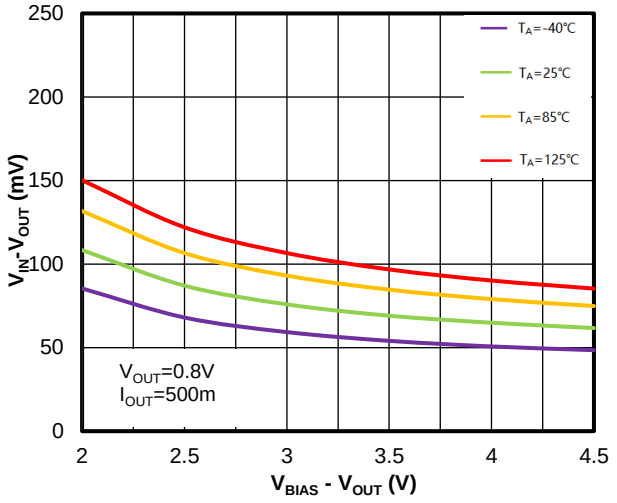


Figure 22. WR0513-ADF16R (0.8V)

IN Dropout Voltage vs. (V_{BIAS} - V_{OUT}) &Ambient Temperature

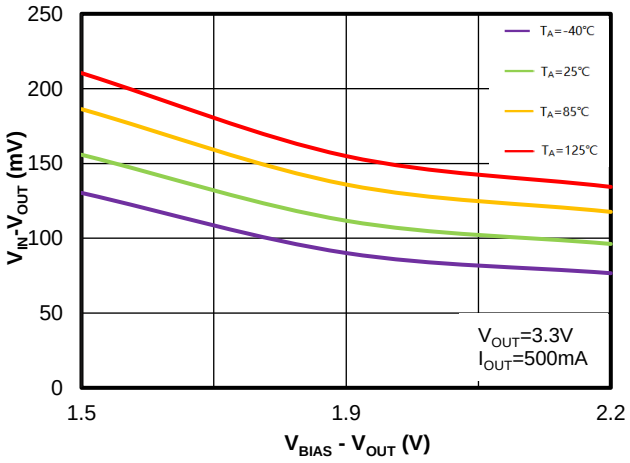


Figure 23. WR0513-ADF16R (3.3V)

IN Dropout Voltage vs. (V_{BIAS} - V_{OUT}) &Ambient Temperature

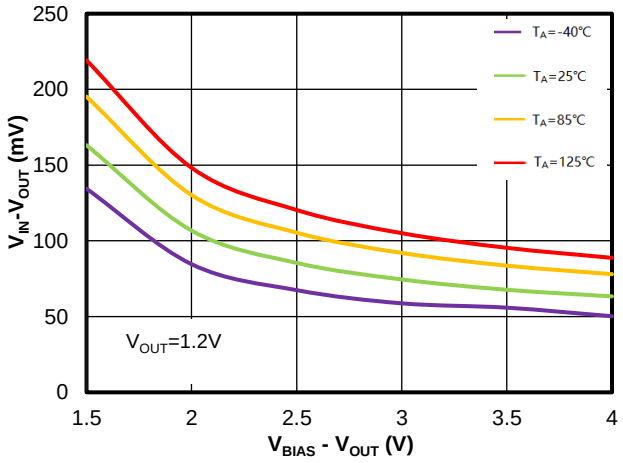


Figure 24. WR0513-12F14R

IN Dropout Voltage vs. (V_{BIAS} - V_{OUT}) &Ambient Temperature

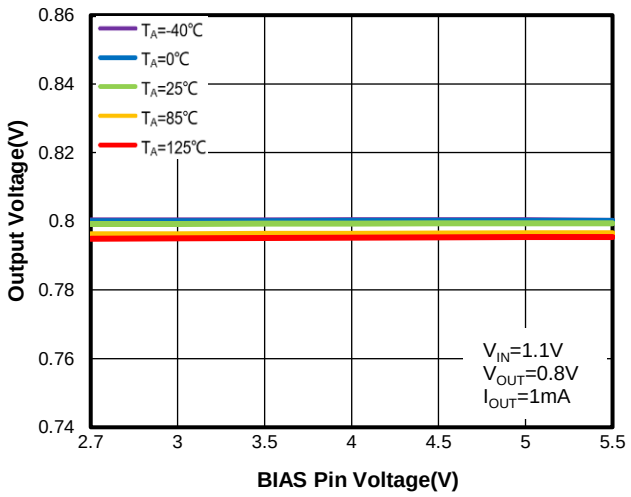


Figure 25. WR0513-ADF16R (0.8V)

Regulation vs. V_{BIAS} & Ambient Temperature

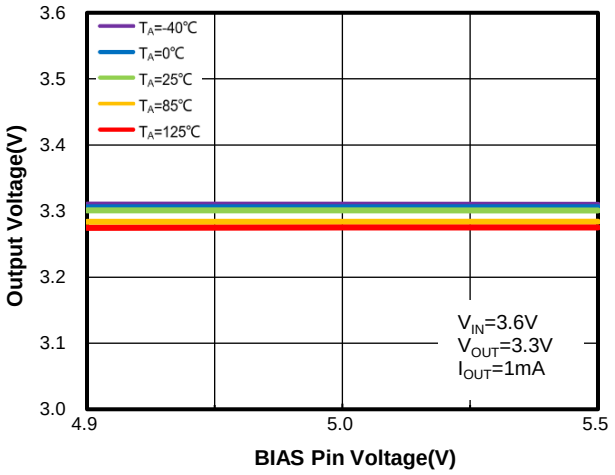


Figure 26. WR0513-ADF16R (3.3V)

Regulation vs. V_{BIAS} & Ambient Temperature

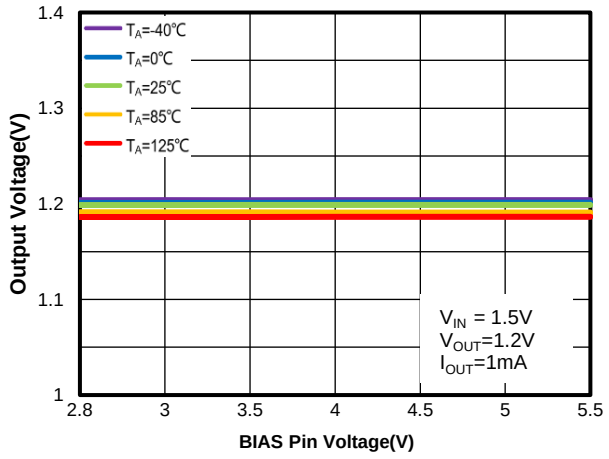


Figure 27. WR0513-12F14R

Regulation vs. V_{BIAS} & Ambient Temperature

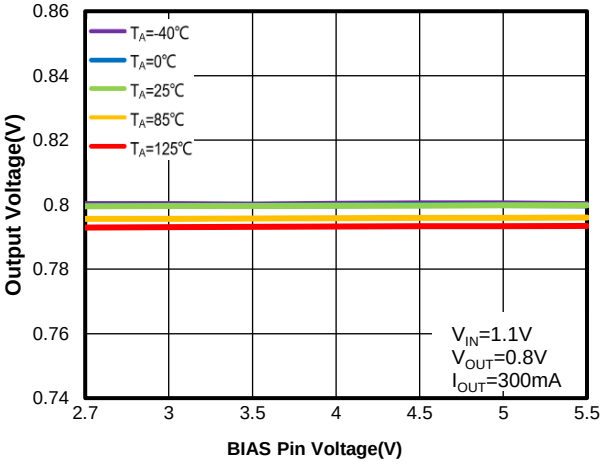


Figure 28. WR0513-ADF16R (0.8V)

Regulation vs. V_{BIAS} & Ambient Temperature

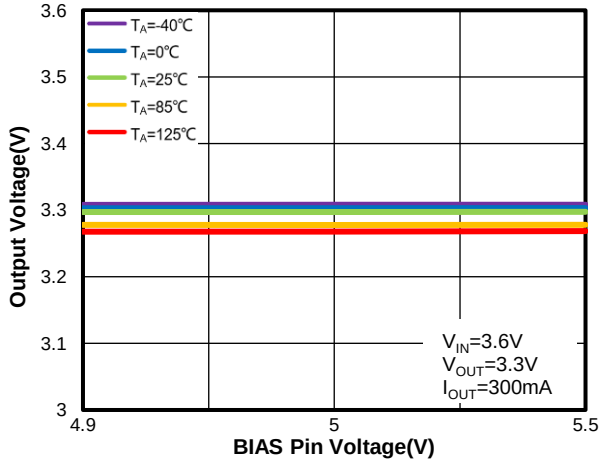


Figure 29. WR0513-ADF16R (3.3V)

Regulation vs. V_{BIAS} & Ambient Temperature

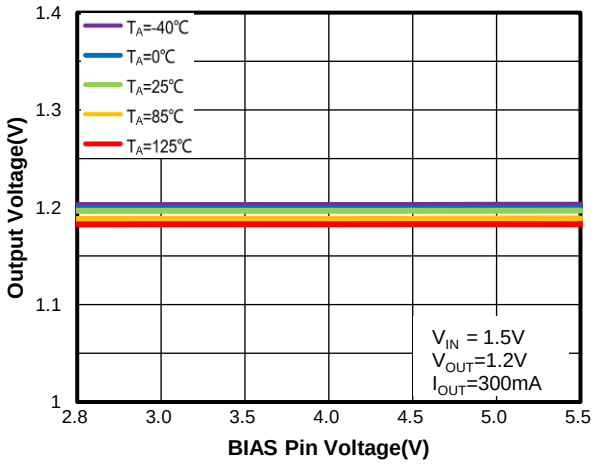


Figure 30. WR0513-12F14R

Regulation vs. V_{BIAS} & Ambient Temperature

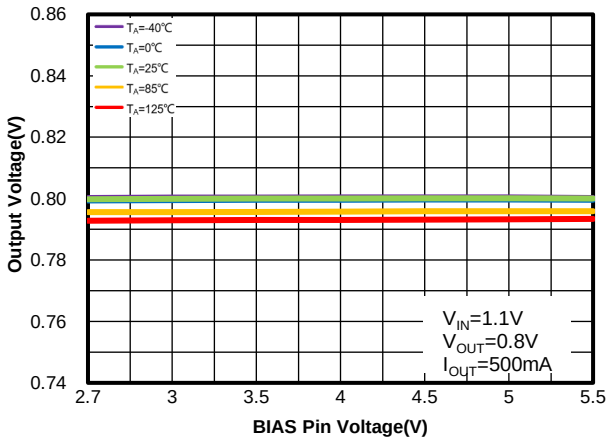


Figure 31. WR0513-ADF16R (0.8V)

Regulation vs. V_{BIAS} & Ambient Temperature

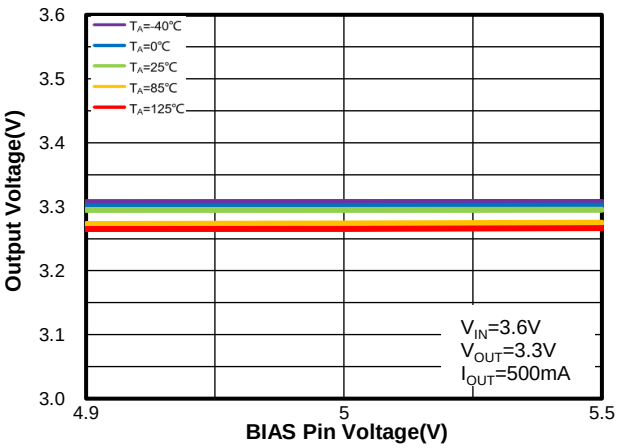


Figure 32. WR0513-ADF16R (3.3V)

Regulation vs. V_{BIAS} & Ambient Temperature

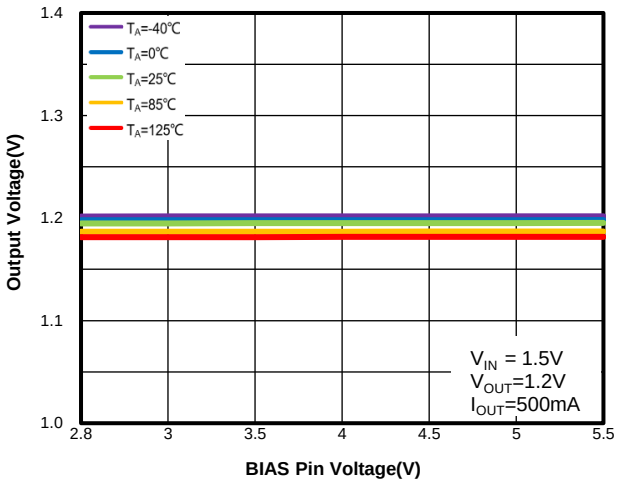


Figure 33. WR0513-12F14R

Regulation vs. V_{BIAS} & Ambient Temperature

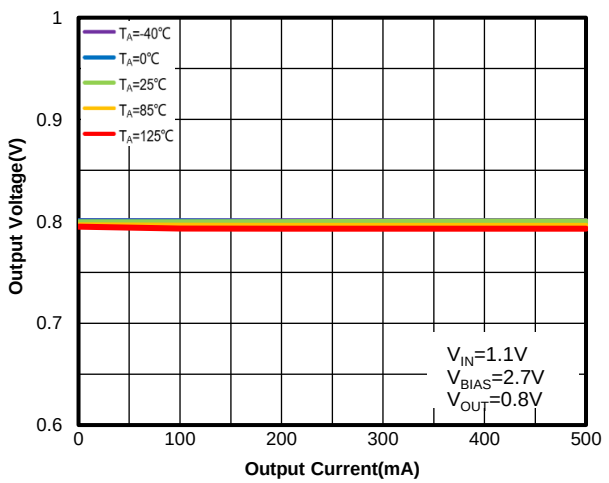


Figure 34. WR0513-ADF16R (0.8V)

Load Regulation vs. I_{OUT} & Ambient Temperature

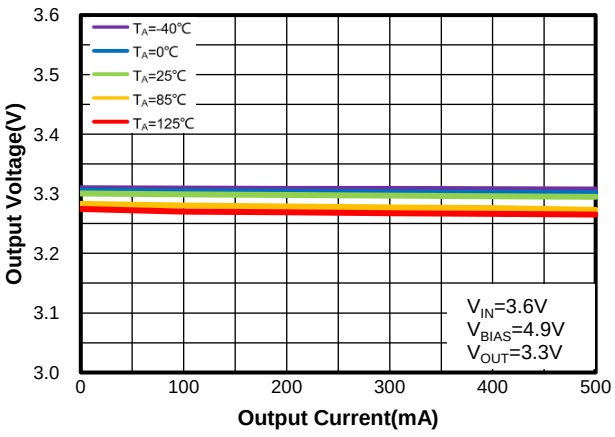


Figure 35. WR0513-ADF16R (3.3V)

Load Regulation vs. I_{OUT} & Ambient Temperature

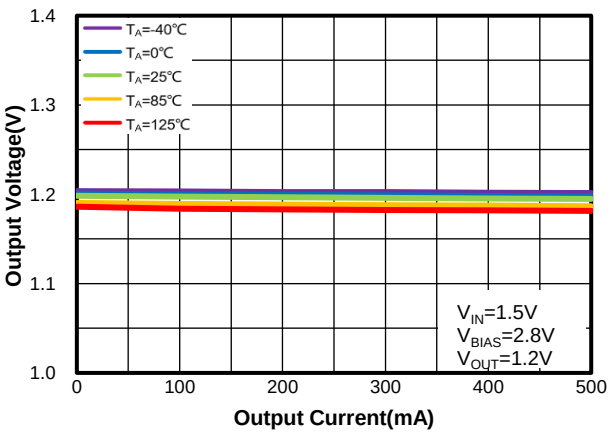


Figure 36. WR0513-12F14R

Load Regulation vs. I_{OUT} & Ambient Temperature

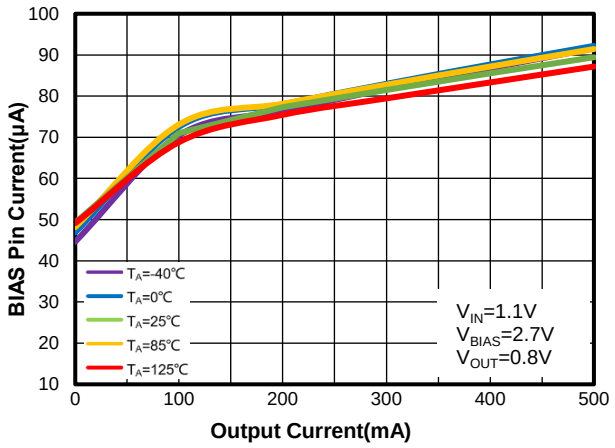


Figure 37. WR0513-ADF16R (0.8V)

BIAS Pin Current vs. I_{OUT} & Ambient Temperature

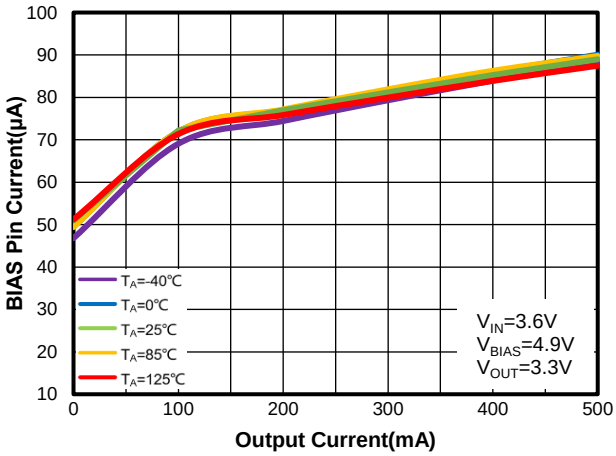


Figure 38. WR0513-ADF16R (3.3V)

BIAS Pin Current vs. I_{OUT} & Ambient Temperature

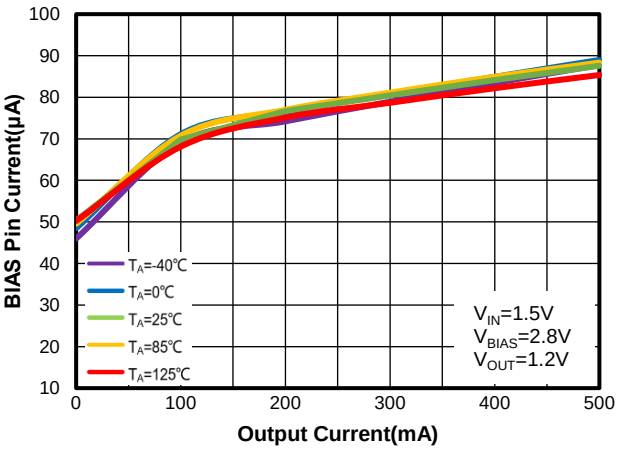


Figure 39. WR0513-12F14R

BIAS Pin Current vs. I_{OUT} & Ambient Temperature

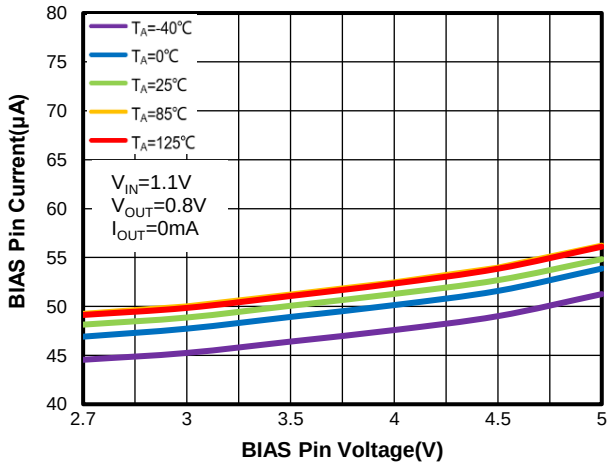


Figure 40. WR0513-ADF16R (0.8V)

BIAS Pin Current vs. V_{BIAS} & Ambient Temperature

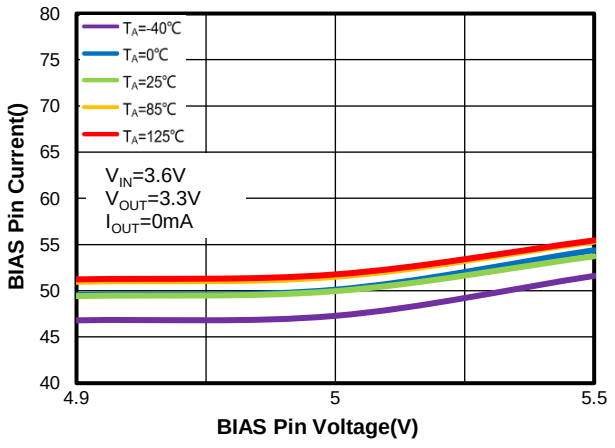


Figure 41. WR0513-ADF16R (3.3V)

BIAS Pin Current vs. V_{BIAS} & Ambient Temperature

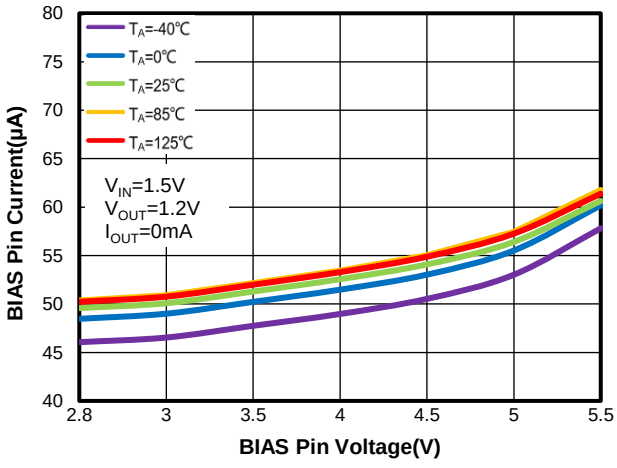


Figure 42. WR0513-12F14R

BIAS Pin Current vs. V_{BIAS} & Ambient Temperature

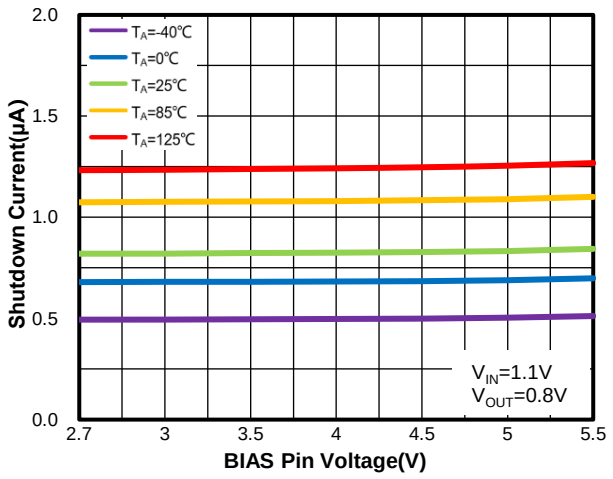


Figure 43. WR0513-ADF16R (0.8V)

Shutdown Current vs. V_{BIAS} & Ambient Temperature

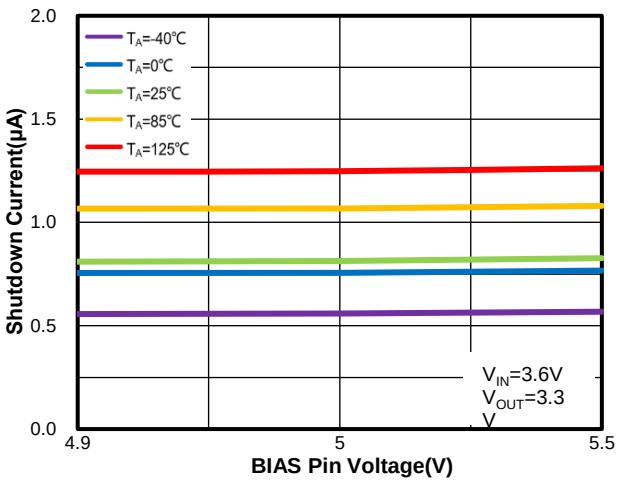


Figure 44. WR0513-ADF16R (3.3V)

Shutdown Current vs. V_{BIAS} & Ambient Temperature

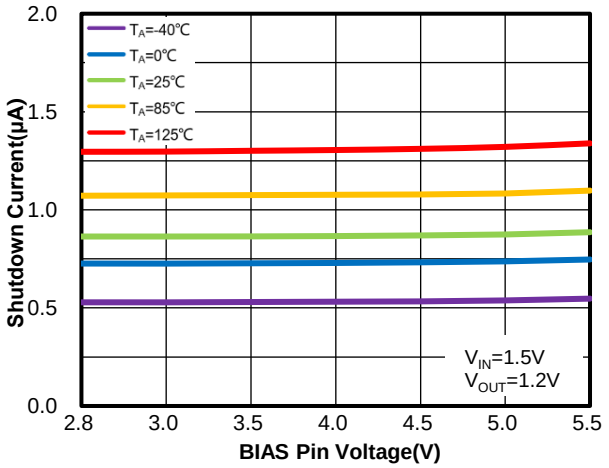


Figure 45. WR0513-12F14R

Shutdown Current vs. V_{BIAS} & Ambient Temperature

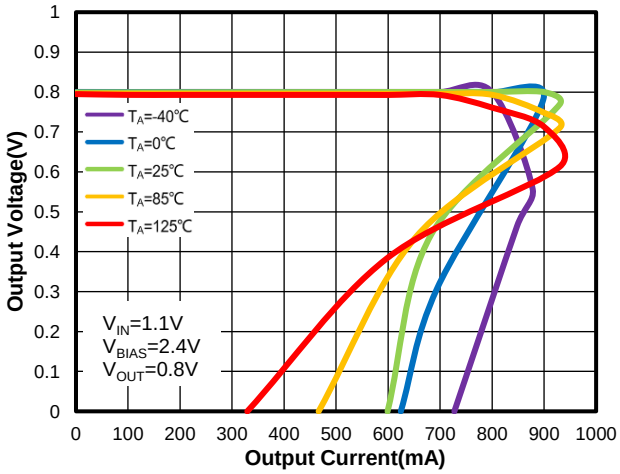


Figure 46. WR0513-ADF16R (0.8V)

Foldback Current Limit vs. I_{OUT} & Ambient Temperature

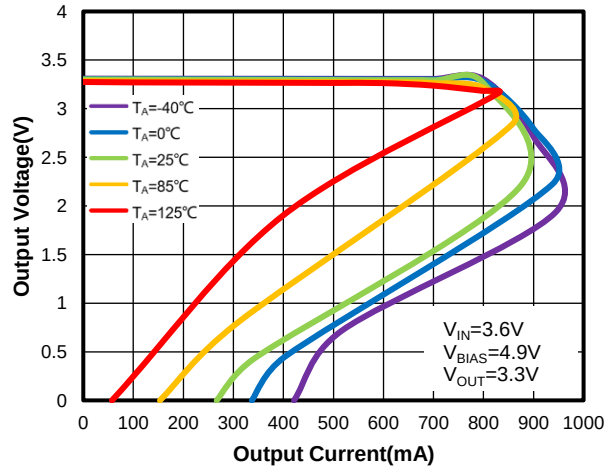


Figure 47. WR0513-ADF16R (3.3V)

Foldback Current Limit vs. I_{OUT} & Ambient Temperature

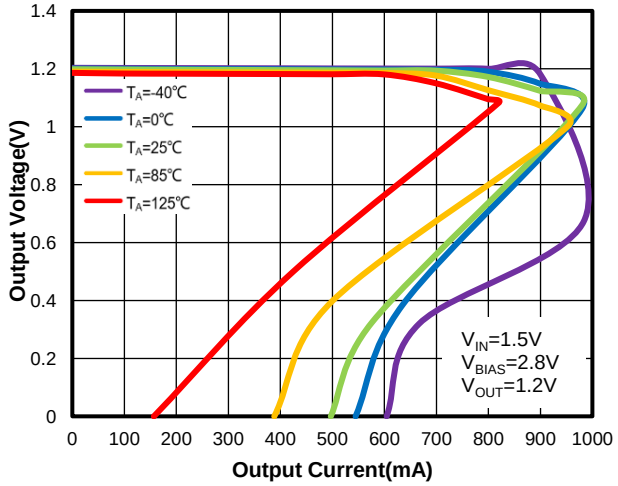


Figure 48. WR0513-12F14R

Foldback Current Limit vs. I_{OUT} & Ambient Temperature

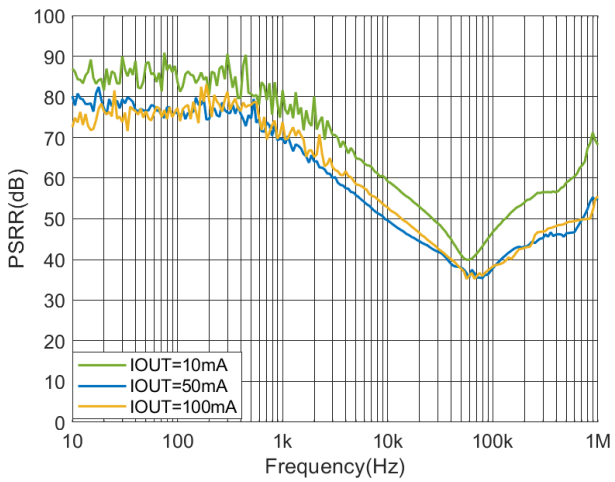


Figure 49. WR0513-12F14R

Power-Supply Rejection Ratio vs. Frequency

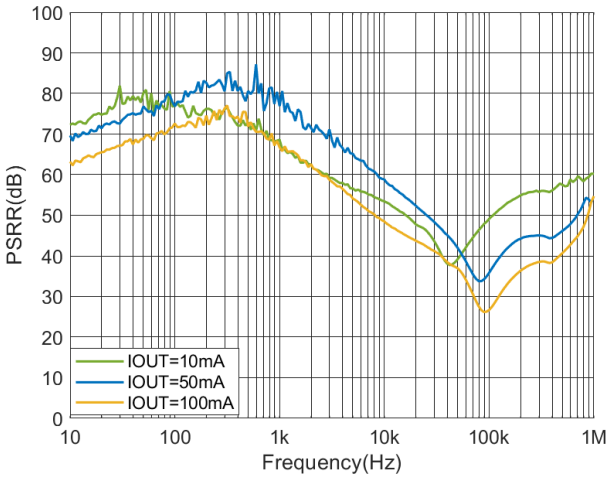


Figure 50. WR0513-18F14R

Power-Supply Rejection Ratio vs. Frequency

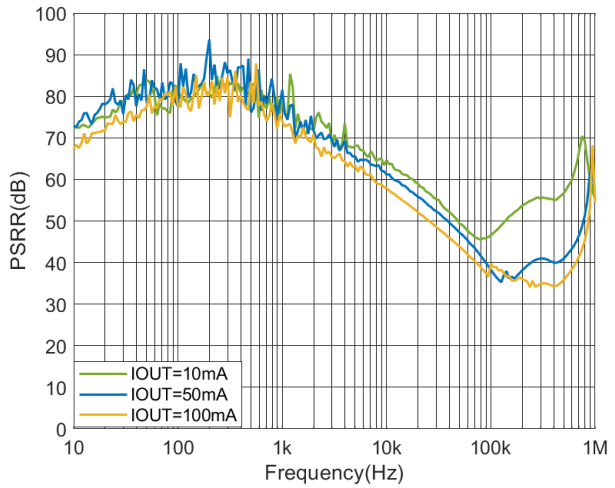


Figure 51. WR0513-28F14R

Power-Supply Rejection Ratio vs. Frequency

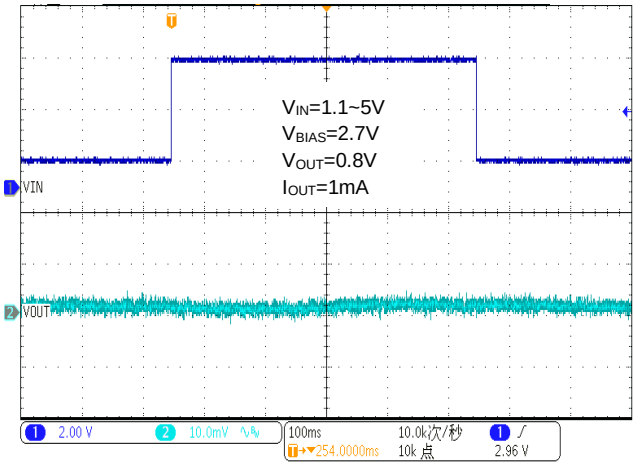


Figure 52. WR0513-ADF16R (0.8V)

Line Transient _ V_{IN}

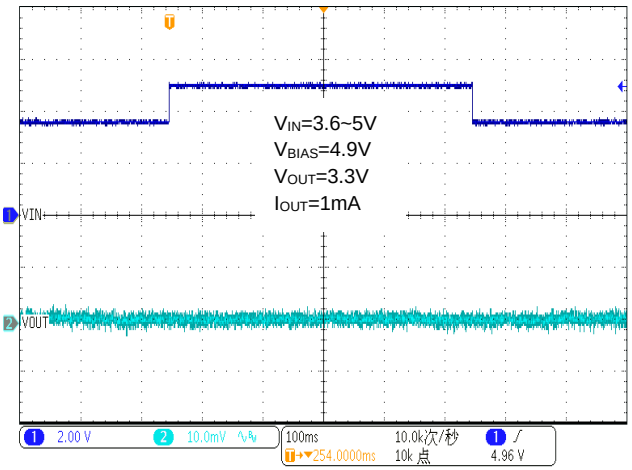


Figure 53. WR0513-ADF16R (3.3V)

Line Transient _ V_{IN}

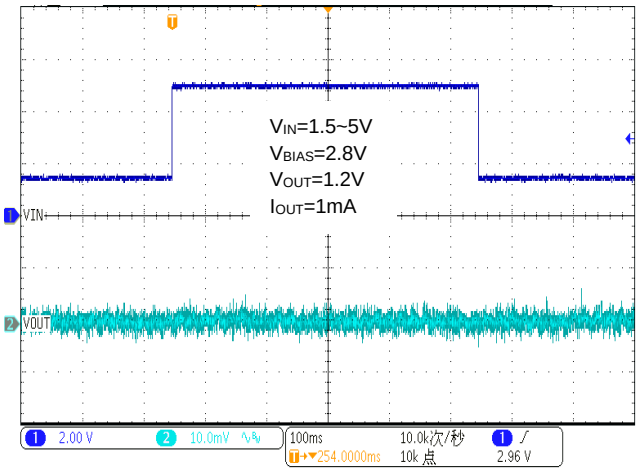


Figure 54. WR0513-12F14R

Line Transient _ V_{IN}

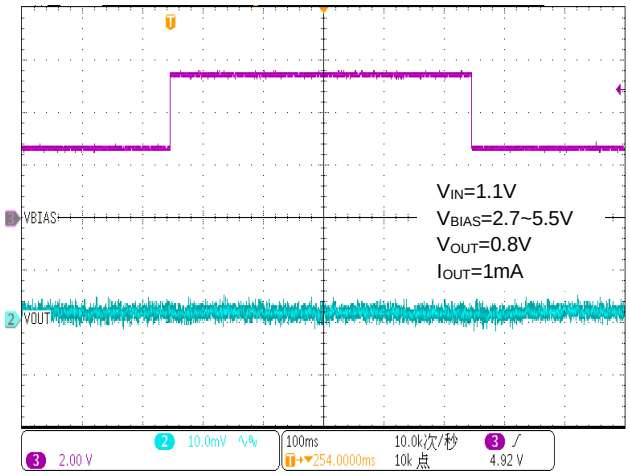


Figure 55. WR0513-ADF16R (0.8V)
Line Transient _ V_{BIAS}

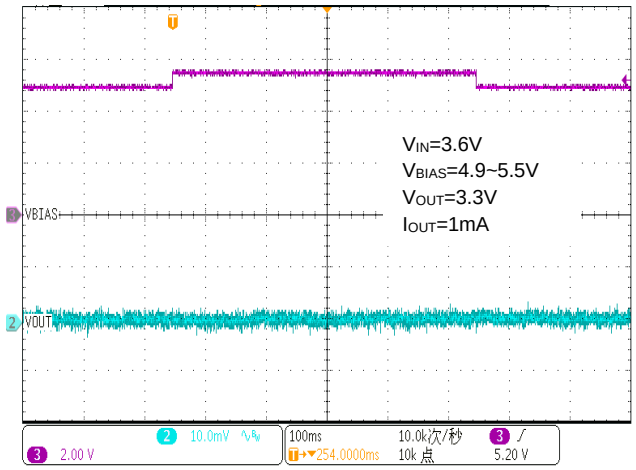


Figure 56. WR0513-ADF16R (3.3V)
Line Transient _ V_{BIAS}

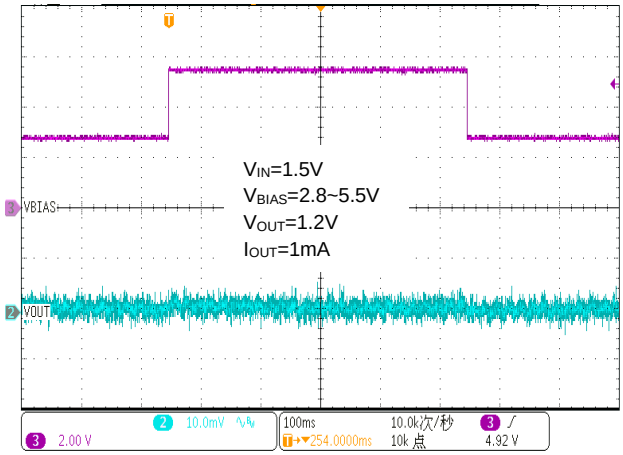


Figure 57. WR0513-12F14R
Line Transient _ V_{BIAS}

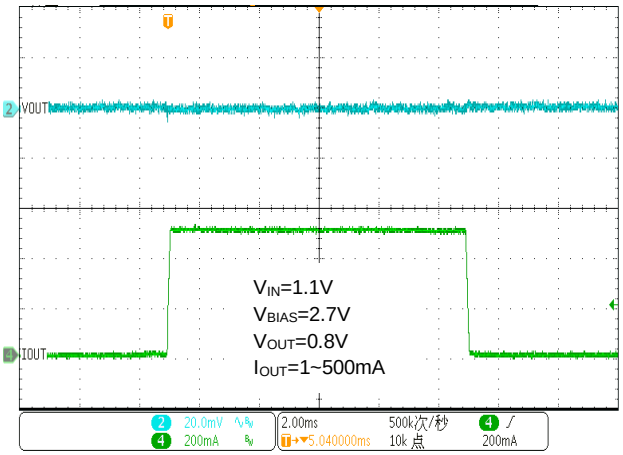


Figure 58. WR0513-ADF16R (0.8V)
Load Transient

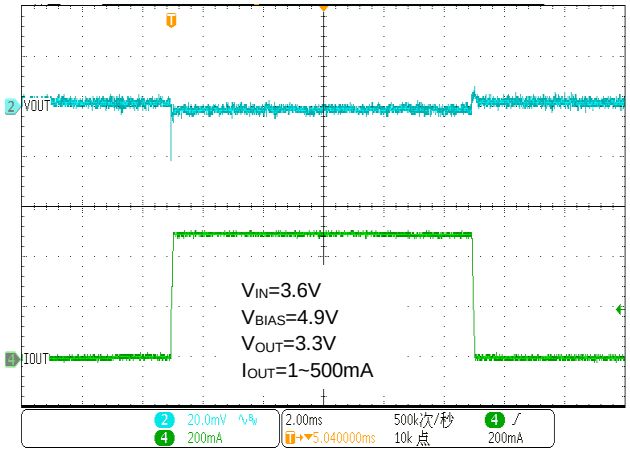


Figure 59. WR0513-ADF16R (3.3V)
Load Transient

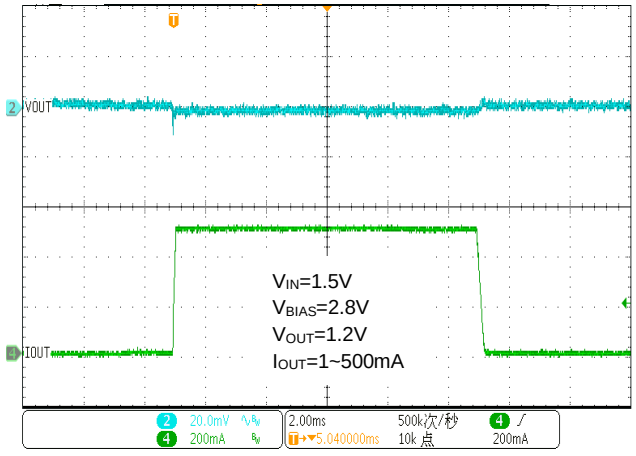


Figure 60. WR0513-12F14R
Load Transient

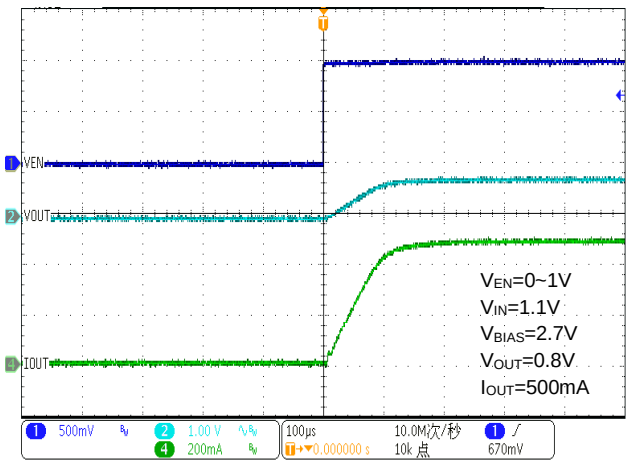


Figure 61. WR0513-ADF16R (0.8V)
Startup with EN

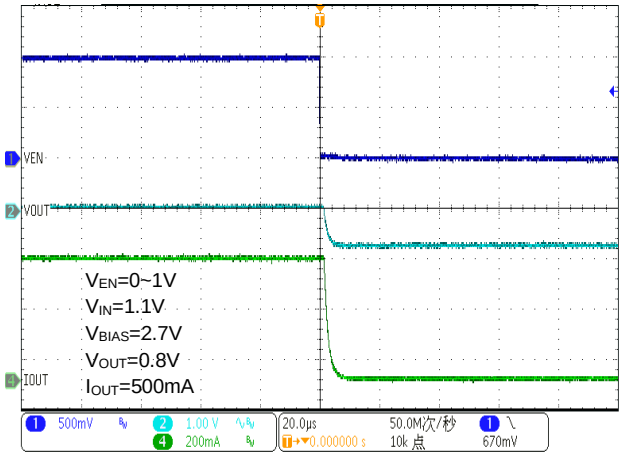


Figure 62. WR0513-ADF16R (0.8V)
EN Shutdown

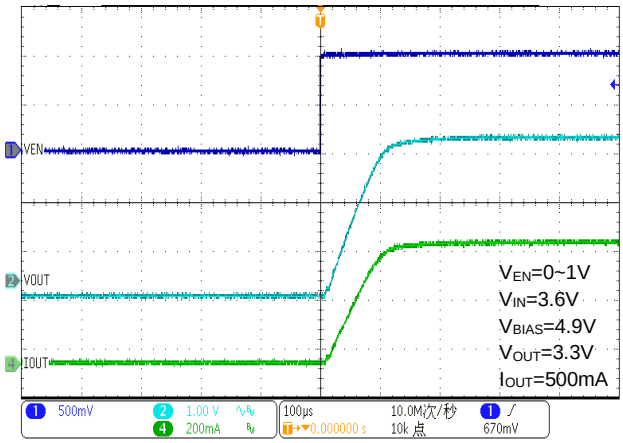


Figure 63. WR0513-ADF16R (3.3V)
Startup with EN

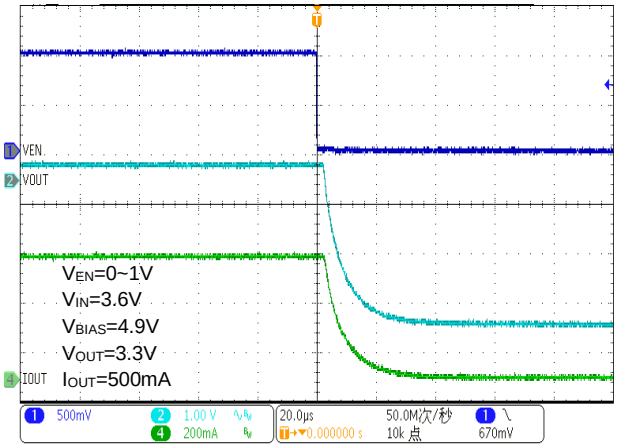


Figure 64. WR0513-ADF16R (3.3V)
EN Shutdown

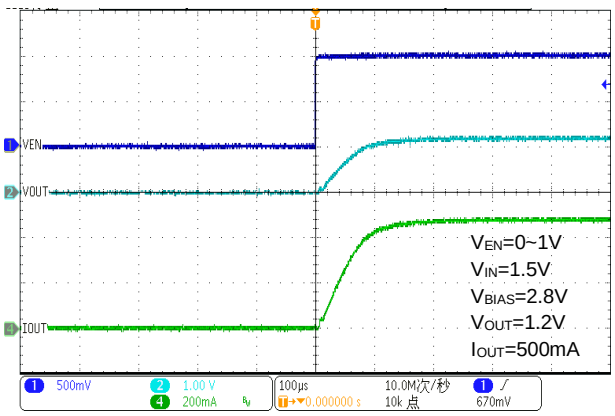


Figure 65. WR0513-12F14R
Startup with EN

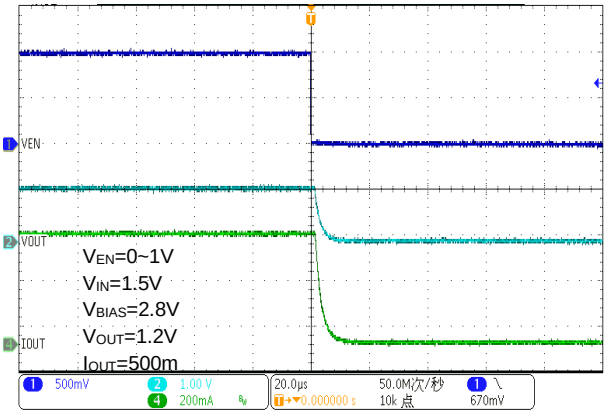


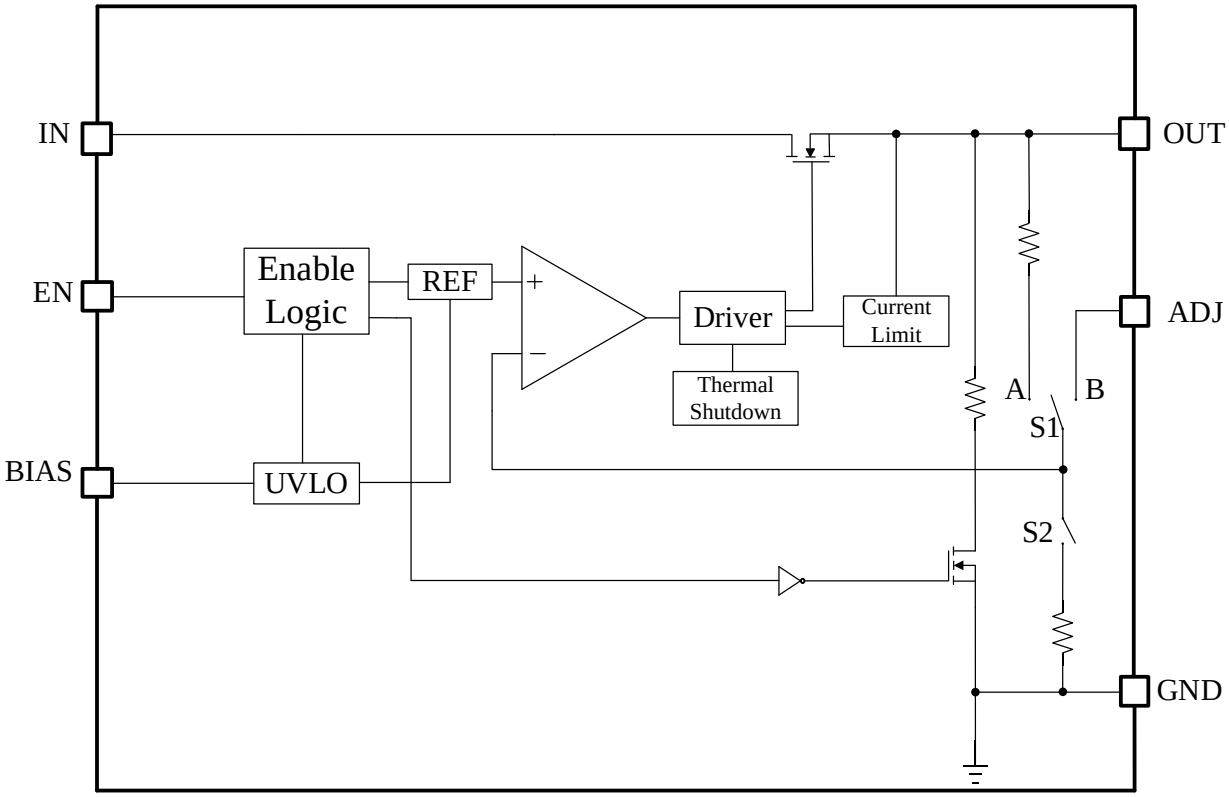
Figure 66. WR0513-12F14R
EN Shutdown

11. Function Description

11.1 Overview

The WR0513 is a 500 mA LDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise and low I_Q suitable for space constrained, noise sensitive applications.

11.2 Block Diagram



NOTE: Fixed version: S1 to A and S2 closed, Adjustable version: S1 to B, S2 open.

11.3 Feature Description

11.3.1 Output Voltage Accuracy

Output voltage accuracy is defined as the maximum and minimum error in output voltage. The errors are introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots. The output voltage accuracy of WR0513 is about 1.5% at T_A = 25℃ and maybe drift in full operating temperature.

11.3.2 Enable (EN)

The WR0513 EN pin has internal pull−down current source with value of 500 nA typ. When the input voltage of the enable pin is higher than the high enable voltage threshold, the device outputs normally. When the input voltage of the enable pin is lower than the low input voltage threshold of the EN pin, the device output shutdown. If you do not need to control the output voltage independently, connect the enable pin to the input of the device.

11.3.3 BIAS Voltage (V_{BIAS})

The V_{BIAS} power supply I_{BIAS} for the LDO control circuit is very low and its input voltage must be above 2.4V or 1.6V above the normal output voltage. V_{BIAS} provides the bias input voltage for the internal error amplifier and reference circuit, which is controlled by the internal undervoltage module. When the bias voltage is greater than the undervoltage threshold, the chip outputs normally; otherwise, the output is abnormal.

11.3.4 Dropout Voltage (V_{DO})

The WR0513 is an ultra-low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the minimum of (V_{IN}-V_{OUT}) at the rated maximum output current where V_{OUT} is the minimum of $V_{OUT(NOM)}$. When the input voltage is below $V_{OUT(NOM)}$ plus V_{DO}, the output voltage varies with the input voltage.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS\ (ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The $R_{DS\ (ON)}$ is calculated by following equation.

$$R_{DS\ (ON)}=V_{DO}/I_{OUT}$$

11.3.5 Power Supply Rejection Ratio (PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

PSRR = 20lg (Ripple(in) / Ripple(out))

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR0513 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.6 Noise

LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is generated inside the electronics; external noise is transmitted from outside the circuit to the internal circuit. The error amplifier determines the PSRR of the LDO and therefore LDO suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimizing noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

The WR0513 has a low noise reference, high PSRR to ensure that output noise is reduced during normal operation.

11.3.7 Foldback Current Limit (I_{LIM})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{LIM}, and when an overload or short circuit occurs, the output current will be maintained at I_{LIM}, and the output voltage will be reduced to $I_{LIM}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{LIM}. The output current is reduced to the set current threshold I_{SHORT} and the output voltage is reduced to $I_{SHORT}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

The WR0513 uses a foldback current limiting mode where the final current is clamped to around 400mA, thus providing good protection to the device.

More information on current limiting can be found in Electrical Characteristics Figure 46 to Figure 48.

11.3.8 Thermal Protection

The WR0513 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 170°C (typical). The thermal shutdown hysteresis ensures that the LDO recover when the temperature drops to 145°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR0513's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR0513 into a thermal shutdown state will reduce the reliability of the device.

11.4 Functional Mode Of The Device

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table belows.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal	$5.5V>V_{IN}>V_{OUT(NOM)}+V_{DROP_IN}$	$5.5V>V_{BIAS}>V_{OUT(NOM)}+V_{DROP_BIAS}$	$V_{EN} > V_{ENH}$	$I_{OUT} < I_{LIM}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(NOM)}+V_{DROP_IN}$	$V_{BIAS} < V_{OUT(NOM)}+V_{DROP_BIAS}$	$V_{EN} > V_{ENH}$	$I_{OUT} < I_{LIM}$	$T_J < T_{SD}$
Disabled	-	$V_{BIAS} < V_{UVLO}$	$V_{EN} < V_{ENL}$	-	$T_J > T_{SD}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(NOM)}$ + V_{DROP_IN}) and is less than 5.5V.
2. The bias voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(NOM)}$ + V_{DROP_BIAS}) and is less than 5.5V.
3. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.
4. The output current is less than the current limit ($I_{OUT} < I_{LIM}$).
5. The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, the device operates in the dropout state and the output voltage tracks the input voltage.

11.4.3 Disabled

The WR0513 can be turned off by forcing the enable pin low, typically with an enable voltage below 0.5V, at which point the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application Guide

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0513 is a linear voltage regulator with an input voltage of 0.8V to 5.5V and an output voltage of 0.6V to 3.6V. The accuracy is 1.5% for V_{REF} voltages. The maximum output current is 500 mA. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Capacitor Recommendation

The WR0513 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN}, V_{BIAS} and V_{OUT} pins to improve their stability. The use of multilayer ceramic capacitors is recommended. These capacitors also have limitations. Ceramic capacitors with X7R-, X5R- and COG grade dielectric materials have relatively good capacitive stability at different temperatures. The WR0513 is designed to use 1μF ceramic capacitors at the input, 0.1μF ceramic capacitors at BIAS and 4.7μF or larger ceramic capacitors at the output. Place C_{IN}, C_{BIAS} and C_{OUT} as close as possible to the IN, BIAS and OUT pins to minimize the tracking inductance from the capacitors to the device.

12.1.2 Power Dissipation (PD)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

P_D can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance ($R_{\theta JA}$) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

The thermal resistance ($R_{\theta JA}$) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.3 Detailed Design Procedure

The adjustable version of WR0513 has a thermally stable reference voltage of 0.8 ± 0.004V， the voltage on the ADJ pin sets the output voltage which is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Lower values for R1 and R2 is recommended to reduce the noise injected from the FB pin. Note that R1 is connected from OUT pin to ADJ pin, and R2 is connected from ADJ to GND.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right)$$

In order to get better load regulation, R1 must be connected very close to the OUT and ADJ pin, while the ground of R2 must be as close as possible to the ground pin of the chip.

Recommended Component Values

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
1.2	12	24
1.8	30	24
2.5	51	24
3.3	75	24

13. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us to get the evaluation module or schematic.

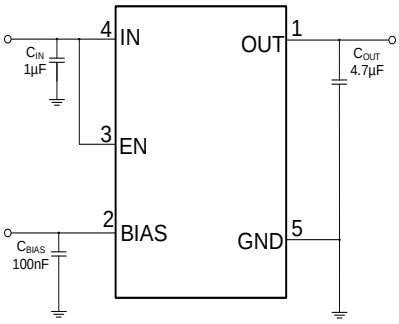
The module names are listed in the following table.

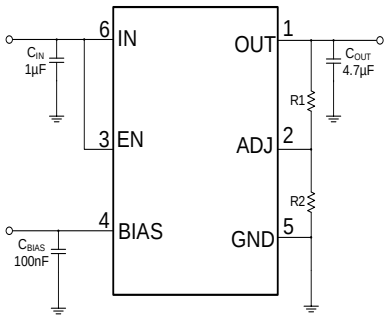
NAME	PACKAGE	EVALUATION MODULE
WR0513	DFN-4L	WAYON LDO EVM V1.0 - DFN1.2×1.2-4L
	DFN-6L	WAYON LDO EVM V1.0 -DFN1.2×1.2-6L

13.1 Typical Application Circuits

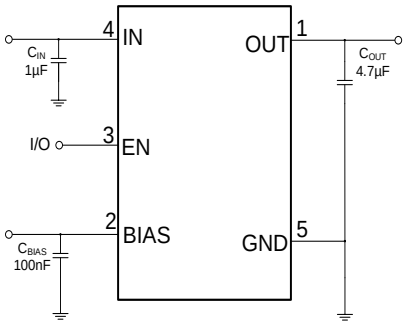
The following figure shows the schematic of the application circuit.

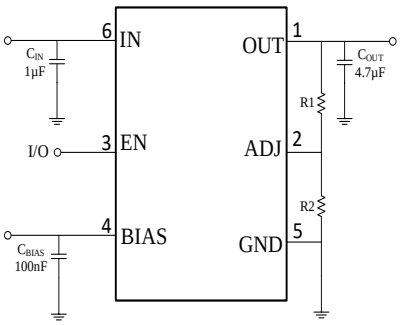
Circuit schematic 1: EN is connected to IN.





Circuit schematic 2: EN is controlled by external voltage.



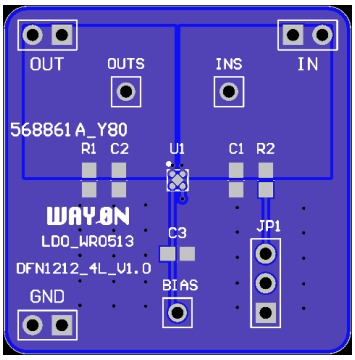


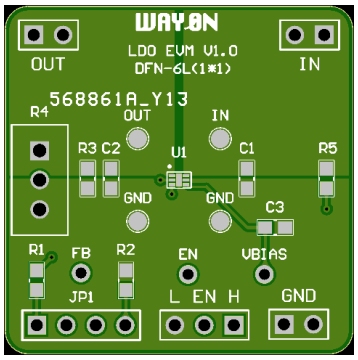
13.2 Layout of Typical Application Circuits

13.2.1 Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. A minimum 1.0μF input capacitor (C_{IN}) is recommended to IN to minimize the effect of resistance and inductance between the source and the LDO input. A minimum 0.1μF input capacitor (C_{BIAS}) is recommended to BIAS and a minimum 4.7μF output capacitor (C_{OUT}) is recommended to OUT. Connect the ground sides of C_{IN} , C_{BIAS} and C_{OUT} with LDO ground pins as close as possible through a wide copper surface. Through-holes and long wires may seriously affect system performance and is not recommended.

13.2.2 Layout Example





14. Naming Conventions

WR AA BB-CC DDD E

W **R:** WAYON Regulator

A **A:** 05 - Output Current 500 mA

B **B:** Serial number

C **C:** Output Voltage/AD-Output Voltage, Adjustable Voltage

DDD: F14- Package, DFN-4

F16- Package, DFN-6

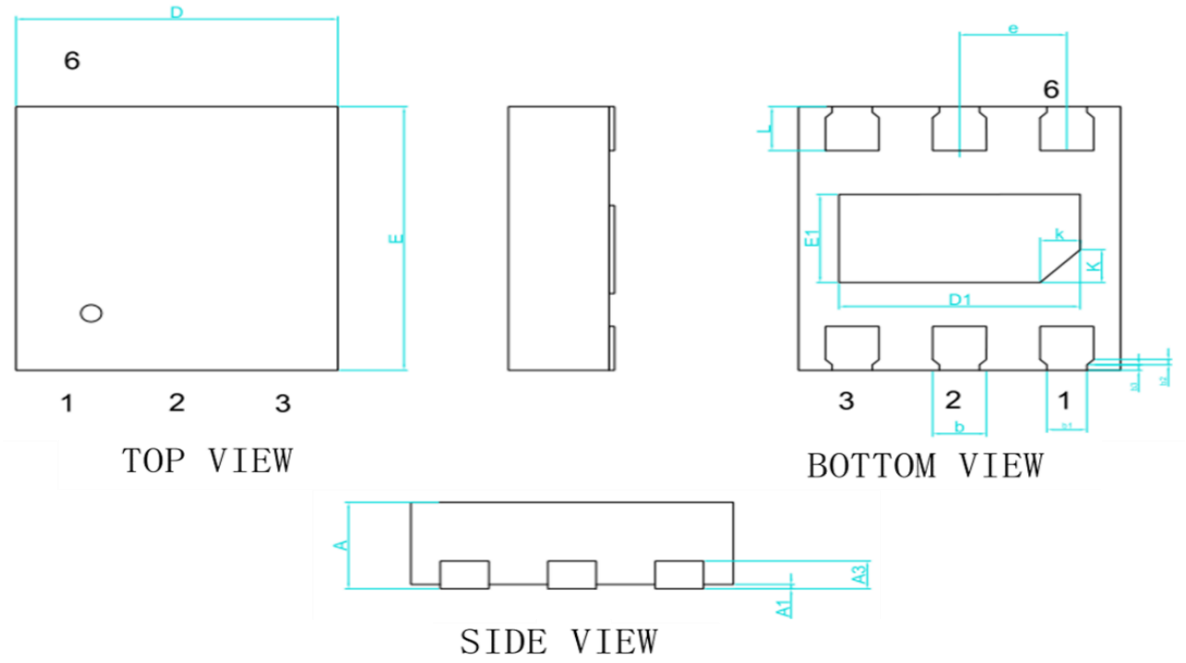
E: R-Reel & T-tube

15. Electrostatic discharge warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

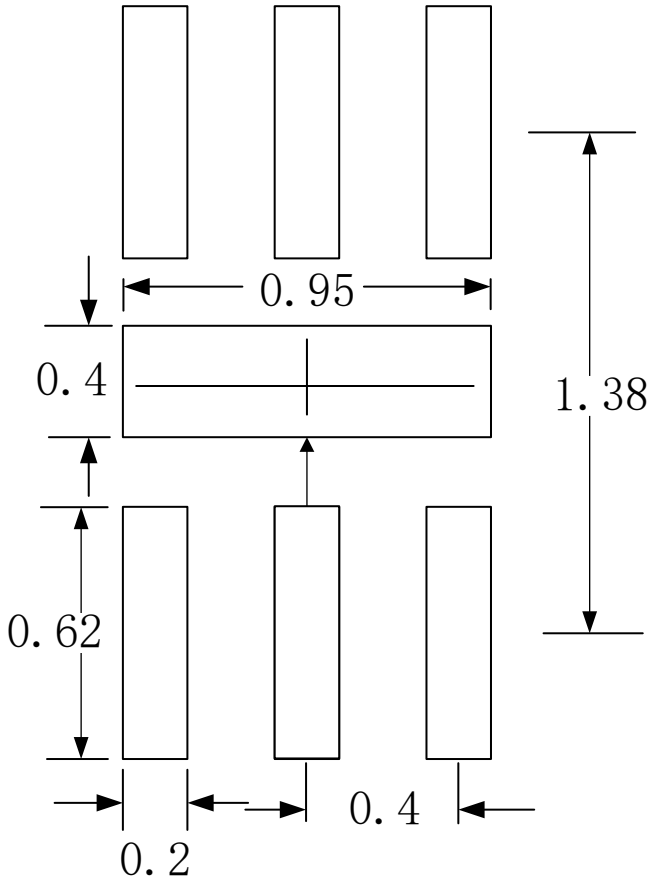
16. Package Information

DFN1.2×1.2-6L



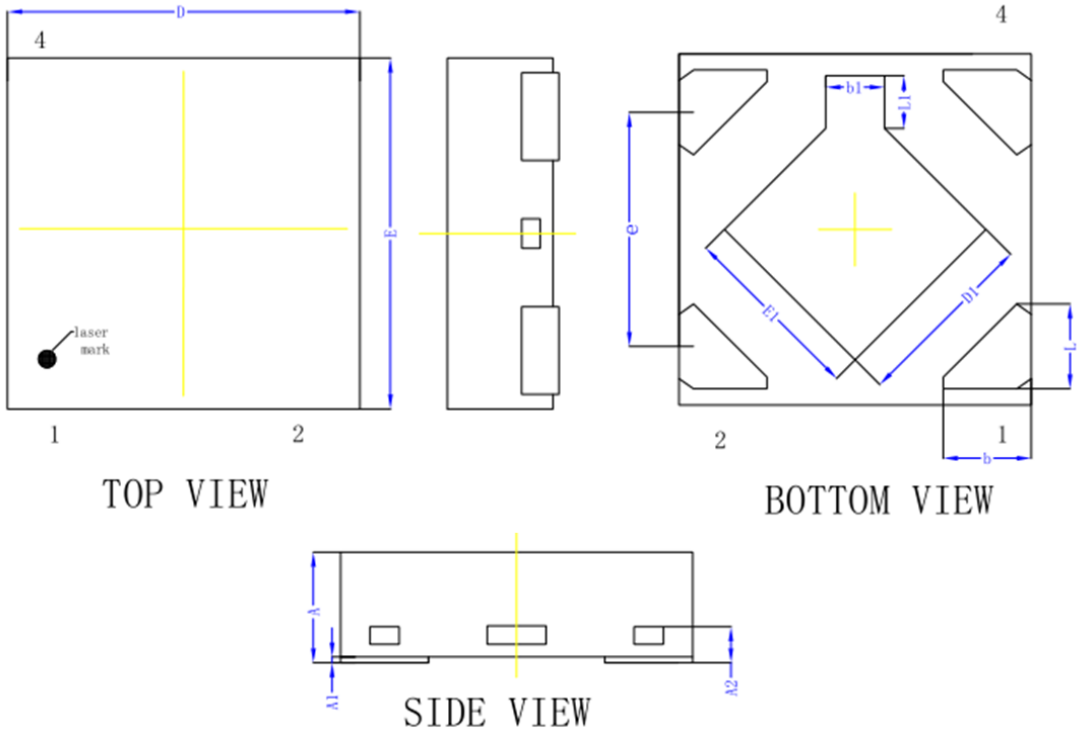
SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	-	0.02
A3		0.127REF	
D	1.15	1.20	1.25
E	1.15	1.20	1.25
D1	0.85	0.95	1.05
E1	0.35	0.40	0.45
k		0.15REF	
e		0.40REF	
b		0.20REF	
b1		0.15REF	
b2		0.025REF	
b3		0.025REF	
L	0.15	0.20	0.25

Recommended Pad Layout: DFN1.2×1.2-6L



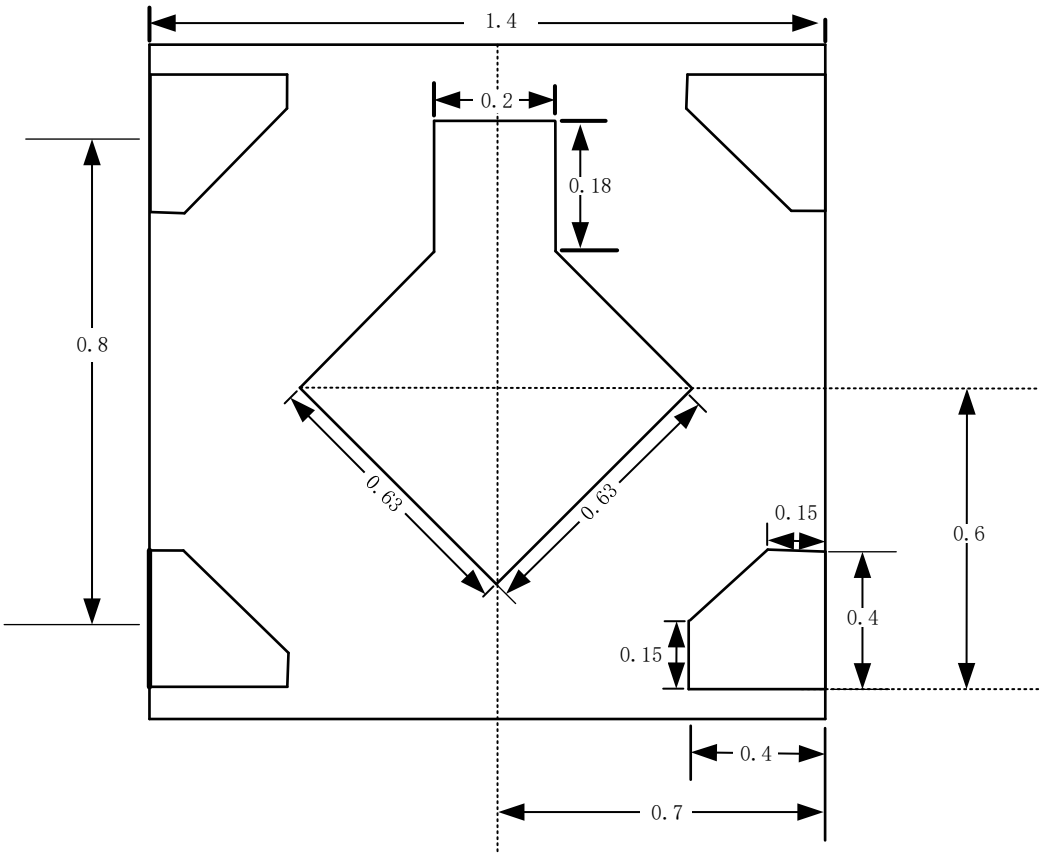
NOTE: Dimensions In Millimeters

DFN1.2×1.2-4L



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MIN
A	0.35	-	0.40
A1	0.00	0.02	0.05
e	0.800BSC		
A2	0.127REF		
D	1.15	1.20	1.25
E	1.15	1.20	1.25
D1	0.58	0.63	0.68
E1	0.58	0.63	0.68
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
L	0.25	0.30	0.35
L1	0.13	0.18	0.23

Recommended Pad Layout: DFN1.2×1.2-4L



NOTE: Dimensions In Millimeters

17. Ordering Information

PART NUMBER	OUTPUT VOLTAGE	PACKAGE	PACKING QUANTITY	MARKING*
WR0513-06F16R	0.6V	DFN1212-6	3k/Reel	513 06
WR0513-08F16R	0.8V	DFN1212-6	3k/Reel	513 08
WR0513-09F16R	0.9V	DFN1212-6	3k/Reel	513 09
WR0513-10F16R	1.0V	DFN1212-6	3k/Reel	513 10
WR0513-105F16R	1.05V	DFN1212-6	3k/Reel	513 105
WR0513-11F16R	1.1V	DFN1212-6	3k/Reel	513 11
WR0513-12F16R	1.2V	DFN1212-6	3k/Reel	513 12
WR0513-15F16R	1.5V	DFN1212-6	3k/Reel	513 15
WR0513-18F16R	1.8V	DFN1212-6	3k/Reel	513 18
WR0513-25F16R	2.5V	DFN1212-6	3k/Reel	513 25
WR0513-28F16R	2.8V	DFN1212-6	3k/Reel	513 28
WR0513-30F16R	3.0V	DFN1212-6	3k/Reel	513 30
WR0513-33F16R	3.3V	DFN1212-6	3k/Reel	513 33
WR0513-ADF16R	Adjustable	DFN1212-6	3k/Reel	513 AD
WR0513-06F14R	0.6V	DFN1212-4	3k/Reel	513 06
WR0513-08F14R	0.8V	DFN1212-4	3k/Reel	513 08
WR0513-09F14R	0.9V	DFN1212-4	3k/Reel	513 09
WR0513-10F14R	1.0V	DFN1212-4	3k/Reel	513 10
WR0513-105F14R	1.05V	DFN1212-4	3k/Reel	513 105

PART NUMBER	OUTPUT VOLTAGE	PACKAGE	PACKING QUANTITY	MARKING*
WR0513-11F14R	1.1V	DFN1212-4	3k/Reel	513 11
WR0513-12F14R	1.2V	DFN1212-4	3k/Reel	513 12
WR0513-125F14R	1.25V	DFN1212-4	3k/Reel	513 125
WR0513-13F14R	1.3V	DFN1212-4	3k/Reel	513 13
WR0513-15F14R	1.5V	DFN1212-4	3k/Reel	513 15
WR0513-18F14R	1.8V	DFN1212-4	3k/Reel	513 18
WR0513-25F14R	2.5V	DFN1212-4	3k/Reel	513 25
WR0513-28F14R	2.8V	DFN1212-4	3k/Reel	513 28
WR0513-30F14R	3.0V	DFN1212-4	3k/Reel	513 30
WR0513-33F14R	3.3V	DFN1212-4	3k/Reel	513 33

Contact Information

No.1001, Shiwan(7) Road, Pudong District, Shanghai, P.R.China.201207
Tel: 86-21-50310888 Fax: 86-21-50757680 Email: market@way-on.com
WAYON website: http://www.way-on.com
For additional information, please contact your local Sales Representative.
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Specifications are subject to change without notice.
The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

Product Specification Statement

- The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.
- The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. WAYON shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and WAYON assumes no responsibility for the application of the product.
- WAYON strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, WAYON cannot guarantee that the information provided in the product specification is entirely accurate and error-free. WAYON shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications. WAYON reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with WAYON to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult WAYON in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.
- Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.
- The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. WAYON shall assume no responsibility for any consequences resulting from such usage.
- Users should also comply with relevant laws, regulations, policies, and standards when using the product specification. Users are responsible for the risks and liabilities arising from the use of the product specification and must ensure that it is not used for illegal purposes. Additionally, users should respect the intellectual property rights related to the product specification and refrain from infringing upon any third-party legal rights. WAYON shall assume no responsibility for any disputes or controversies arising from the above-mentioned issues in any form.