1. General Description

The WR1241 is a 4-channel LDO PMIC for camera applications including 2-channel high efficiency and ultra-low DVDD, 2-channel high PSRR and low noise AVDD. Due to low voltage and high current of DVDD, WR1241 uses N-MOSFET architecture without charge pump for 2-channel DVDD. VIN1 is the input source and VIN2 is the bias voltage for 2-channel DVDD. For the AVDD, WR1241 uses P-MOSFET architecture, the input source is VIN2. With 400kHz high speed I²C interface, the function setting is flexible such as power sequence, output voltage, output discharge. The chip enables control supporting EN pin control and I²C control.

The WR1241 regulators are available in DFN2×2-10L package. Standard products are Pb-free and halogen-free.

2. Features

- VIN1 input voltage range: 0.6V to 2.0V
- VIN2 input voltage range: 3V to 5.5V
- VIN2 UVLO voltage: 2V
- VIN2 quiescent current: 65μA
- VIN2 shutdown current: 0.25μA
- DVDD1/2 output voltage range: 0.6V to 1.8V
- DVDD1/2 dropout voltage: 100mV@0.8A
- DVDD1/2 output current capability: 1.2A
- AVDD1/2 output voltage range: 1.2V to 4.3V
- AVDD1/2 dropout voltage: 100mV@0.3A
- AVDD1/2 output current capability: 0.4A
- AVDD1/2 PSRR: 90dB@1kHz
- AVDD1/2 noise: 10μVrms

3. Applications

- Camera Sensor
- Camera Module
- Digital Camera
- Smart Phone
- Security Equipment

4. Typical Application

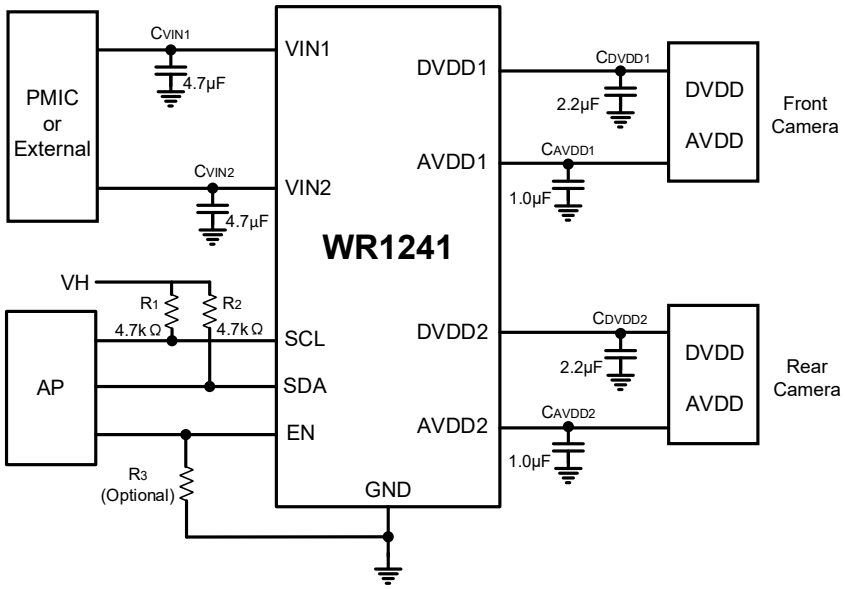
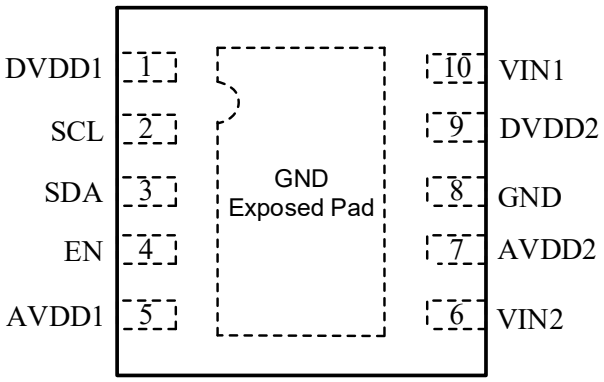


Figure 1 Simplified Schematic

5. Pin Configuration

(Top View)



DFN2×2-10L

6. Pin Description

PIN NUMBER	PIN NAME	I/O	PIN FUNCTION
1	DVDD1	O	LDO1 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.
2	SCL	-	I^2C clock interface.
3	SDA	-	I^2C data interface.
4	EN	-	Enable Pin. Set EN pin high to turn on the regulator. Set EN pin low to turn off the regulator. Keep this pin low if I^2C control is used.
5	AVDD1	O	LDO3 output. Connecting a 1.0μF or more ceramic capacitor at the output pin.
6	VIN2	I	LDO1 and LDO2 VBIAS input pin, LDO3 and LDO4 power supply input pin. Connecting a 4.7μF or more ceramic capacitor at the input pin.
7	AVDD2	O	LDO4 output. Connecting a 1.0μF or more ceramic capacitor at the output pin.
8	GND	-	Ground pin.
9	DVDD2	O	LDO2 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.
10	VIN1	I	LDO1 and LDO2 power supply input pin. Connecting a 4.7μF or more ceramic capacitor at the input pin.

7. Absolute Maximum Ratings [1]

SYMBOL	PARAMETER	RATING	UNIT
V_{VIN1}, V_{VIN2}	VIN1, VIN2 Voltage	-0.3 to 6.5	V
V_{EN}	EN Voltage	-0.3 to (V_{IN} + 0.3)	V
V_{DVDD1}, V_{DVDD2}, V_{AVDD1}, V_{AVDD2}	DVDD1, DVDD2, AVDD1, AVDD2 Voltage	-0.3 to (V_{IN} + 0.3)	V
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance	71.1	℃/W
T_J	Junction Temperature	-40 to 125	℃
T_{STG}	Storage Temperature	-55 to 150	℃
T_{SDR}	Lead Temperature (Soldering, 10 sec)	260	℃
V_{ESD}	ESD Rating HBM all pins	2000	V

NOTE1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN1}	Input Voltage	0.6	2.0	V
V_{IN2}	Input Voltage	3	5.5	V
$I_{OUT(DVDD1/2)}$	Output Current Range	0	1200	mA
$I_{OUT(AVDD1/2)}$	Output Current Range	0	400	mA
$C_{VIN1/2}$	Input capacitor	4.7		μF
$C_{DVDD1/2}$	Output capacitor	2.2		μF
$C_{AVDD1/2}$	Output capacitor	1.0		μF
T_A	Operating Ambient Temperature	-40	85	℃

9. Electrical Characteristics

(V_{IN1} =1.5 V, V_{IN2} =3.3 V, V_{EN} = 1.2 V, I_{OUT}=1mA, $C_{VIN1/2}$=4.7μF, $C_{DVDD1/2}$=2.2μF, $C_{AVDD1/2}$=1.0μF, T_A=25°C, unless otherwise noted)[1] [2] [3]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Whole device						
I_{SHDN}	Shutdown Current	V_{EN}=0V or disabled by I^2C		0.25	1	μA
I_Q	Quiescent Current[4]	V_{EN}=1.2V or all channels enabled by I^2C		65		μA
R_{EN}	EN Pull Down Resistance	V_{EN}=0V to 5.5V		10		MΩ
V_{ENH}	EN Input Logic-High Voltage	-40°C≤T_A≤85°C	1.1			V
V_{ENL}	EN Input Logic-Low Voltage	-40°C≤T_A≤85°C			0.4	V
R_{DISCH}	Auto Discharge Resistance	EN<0.4V, I_{OUT}=0mA for AVDD		400		Ω
		EN<0.4V, I_{OUT}=0mA for DVDD		480		Ω
V_{UVLO}	Under Voltage Lock-out	V_{IN2} Falling		2.0		V
V_{UVLO_HYS}	UVLO Hysteresis	V_{IN2} Rising		0.1		V
T_{SHDN}	Thermal Shutdown Threshold	Temperature Rising		155		°C
$\triangle T_{SD}$	Thermal shutdown hysteresis	Temperature Falling		30		°C
LDO1, LDO2 (DVDD1/2)						
V_{IN1_RANGE}	Input Supply Range		0.6		2.0	V
V_{OUT_ACC}	Output Voltage Accuracy		-2		2	%
V_{OUT_RANGE}	Output Voltage Range		0.6		1.8	V
$V_{OUT\ DEFAULT}$	Default Output Voltage			1.2		V
LDR	Load Regulation	1mA≤ I_{OUT}≤ 1.2A		1		mV
LNR	Line Regulation	V_{IN2}=3.3V,1.25V≤V_{IN1}≤2V, I_{OUT}=1mA		0.1		mV
		V_{IN1}=1.35V, 3V≤V_{IN2}≤4V, I_{OUT}=1mA		0.5		mV

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
V_{DROP}	Dropout Voltage [5]	I_{OUT}=0.8A, $V_{OUT(SET)}$=1.2V, V_{IN2}=3.3V			120		mV
		I_{OUT}=0.8A, $V_{OUT(SET)}$=1.2V, V_{IN2}=4.4V			100		mV
PSRR	Power Supply Ripple Rejection[6]	I_{OUT}=10mA, f=1kHz, V_{IN1}=1.7V+0.2V_{PP}, V_{IN2}=4.4V, $V_{OUT(SET)}$=1.2V			71		dB
		I_{OUT}=10mA, f=1kHz, V_{IN2}=4.4V+0.2V_{PP}, V_{IN1}=1.35V, $V_{OUT(SET)}$=1.2V			47		dB
V_N	Output Voltage Noise	I_{OUT}=30mA, BW=10Hz to 100kHz			90		μVrms
I_{CL}	Output Current Limit	DVDD1	DVDD2				
		REG01[1:0]= 00 (default)	REG01[3:2]= 00 (default)	1000	1300		mA
		REG01[1:0]= 01	REG01[3:2]= 01	1100	1440		mA
		REG01[1:0]= 10	REG01[3:2]= 10	1200	1580		mA
		REG01[1:0]= 11	REG01[3:2]= 11	1300	1720		mA
I_{SC}	Short Current Limit	V_{OUT}=0V			500		mA
V_{TC}	Output Voltage Temperature Coefficient	-40°C ≤T_A≤85°C			±50		ppm/°C
LDO3, LDO4 (AVDD1/2)							
V_{IN2_RANGE}	Input Supply Range			3		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy			-2		2	%
V_{OUT_RANGE}	Output Voltage Range			1.2		4.3	V
$V_{OUT\ DEFAULT}$	Default Output Voltage				2.8		V
LDR	Load Regulation	1mA≤I_{OUT}≤400mA V_{IN1}=1.35V, V_{IN2}=3.3V, $V_{OUT(SET)}$=2.8V			2		mV
LNR	Line Regulation	V_{IN1}=1.35V, I_{OUT}=1mA, $V_{OUT(SET)}$=2.8V, 3.0V≤V_{IN2} ≤4.0V			0.1		mV

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
V_{DROP}	Dropout Voltage [5]	I_{OUT}=300mA, $V_{OUT(SET)}$=2.8V			100		mV
PSRR	Power Supply Ripple Rejection [6]	I_{OUT}=50mA, f=1kHz, V_{IN2}=4.4V+0.2V_{PP}, V_{IN1}=1.35V, $V_{OUT(SET)}$=2.8V			90		dB
		I_{OUT}=50mA, f=1MHz, V_{IN2}=4.4V+0.2V_{PP}, V_{IN1}=1.35V, $V_{OUT(SET)}$=2.8V			38		dB
V_N	Output Voltage Noise	IOUT=30mA, BW=10Hz to 100kHz			10		μVrms
I_{CL}	Output Current Limit	AVDD1	AVDD2				
		REG01[5:4]= 00 (default)	REG01[7:6]= 00 (default)	300	480		mA
		REG01[5:4]= 01	REG01[7:6]= 01	400	620		mA
		REG01[5:4]= 10	REG01[7:6]= 10	500	760		mA
		REG01[5:4]= 11	REG01[7:6]= 11	600	900		mA
I_{SC}	Short Current Limit	V_{OUT}=0V			200		mA
V_{TC}	Output Voltage Temperature Coefficient	-40°C ≤ T_A ≤ 85°C			±50		ppm/°C
I²C Interface Timing (FAST MODE)							
f_{SCL}	Interface clock frequency				400		kHz
$t_{HD:STA}$	(Repeat-start) Start condition hold time			0.6			μs
$t_{SU:STA}$	(Repeat-start) Start condition setup time			0.6			μs
t_{LOW}	Low level width of SCL			1.3			μs
t_{HIGH}	High level width of SCL			0.6			μs
$t_{HD:DAT}$	Data hold time			0			μs
$t_{SU:DAT}$	Data setup time			0.1			μs
t_R	Rising time of SDA and SCL					0.3	μs

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
t_F	Falling time of SDA and SCL				0.3	μs
$t_{SU:STO}$	Stop condition setup time		0.6			μs
t_{BUF}	Time between start and stop condition		1.3			μs
I²C Interface Timing (FAST MODE PLUS)						
f_{SCL}	Interface clock frequency			1000		kHz
$t_{HD:STA}$	(Repeat-start) Start condition hold time		0.26			μs
$t_{SU:STA}$	(Repeat-start) Start condition setup time		0.26			μs
t_{LOW}	Low level width of SCL		0.5			μs
t_{HIGH}	High level width of SCL		0.26			μs
$t_{HD:DAT}$	Data hold time		0			μs
$t_{SU:DAT}$	Data setup time		0.05			μs
t_R	Rising time of SDA and SCL				0.12	μs
t_F	Falling time of SDA and SCL				0.12	μs
$t_{SU:STO}$	Stop condition setup time		0.26			μs
t_{BUF}	Time between start and stop condition		0.5			μs

NOTE1: All voltages are with respect to the device GND terminal, unless otherwise stated.

NOTE2: Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.

NOTE3: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application $R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$. See Application and Implementation.

NOTE4: Quiescent current is defined here as the difference in current between the input voltage source and the load at VOUT.

NOTE5: Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

NOTE6: This specification is verified by design.

10. Test Circuit

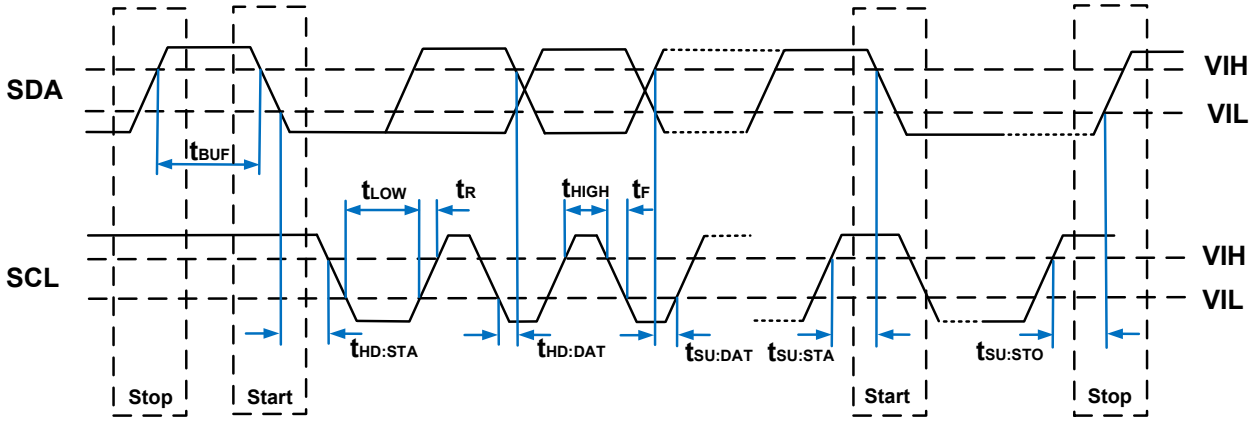


Figure 2 I²C Timing Diagram

11. Typical Performance Characteristics

(V_{IN} =$V_{OUT(SET)}$+1V, V_{EN} = 1.2 V, I_{OUT}=1mA, $C_{VIN1/2}$=4.7μF, $C_{DVDD1/2}$=2.2μF, $C_{AVDD1/2}$=1.0μF, T_A=25°C, unless otherwise noted)

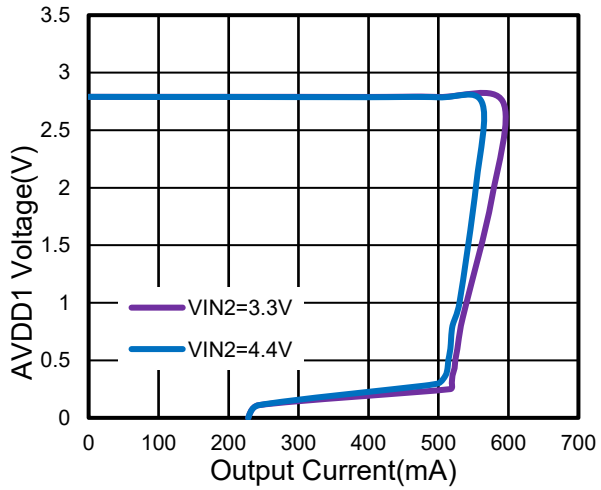


Figure 3. AVDD1 Voltage vs. Output Current

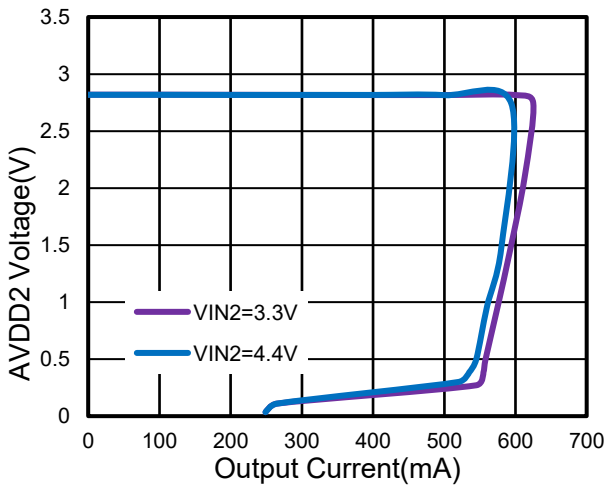


Figure 4. AVDD2 Voltage vs. Output Current

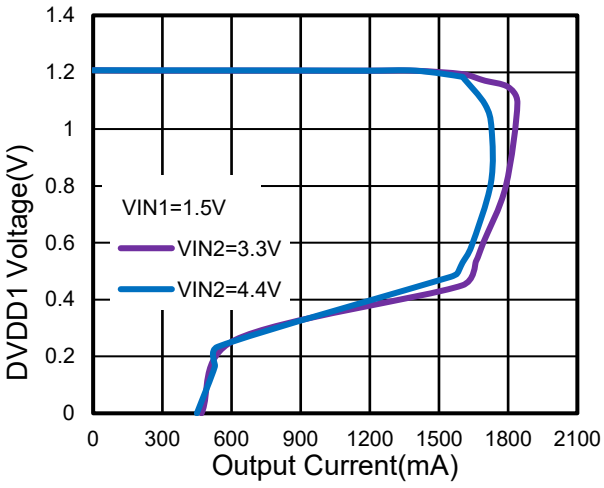


Figure 5. DVDD1 Voltage vs. Output Current

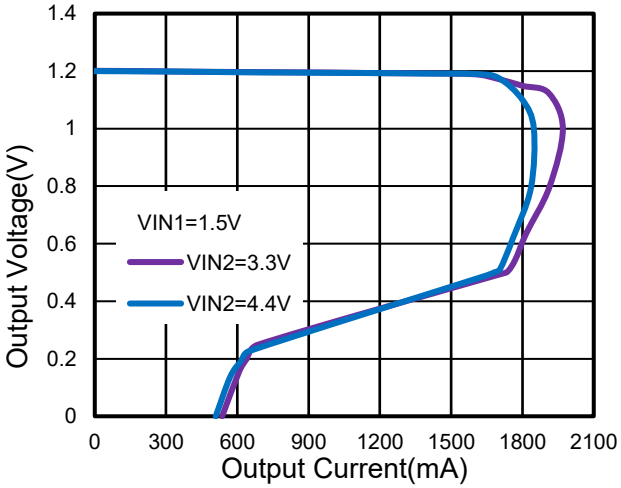


Figure 6. DVDD2 Voltage vs. Output Current

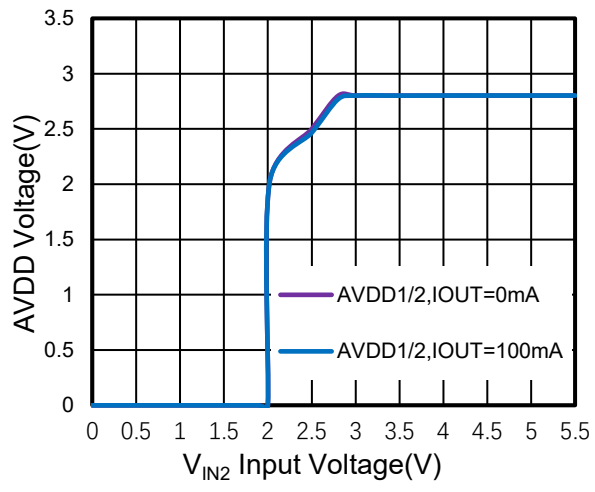


Figure 7 AVDD Voltage vs. Input Voltage

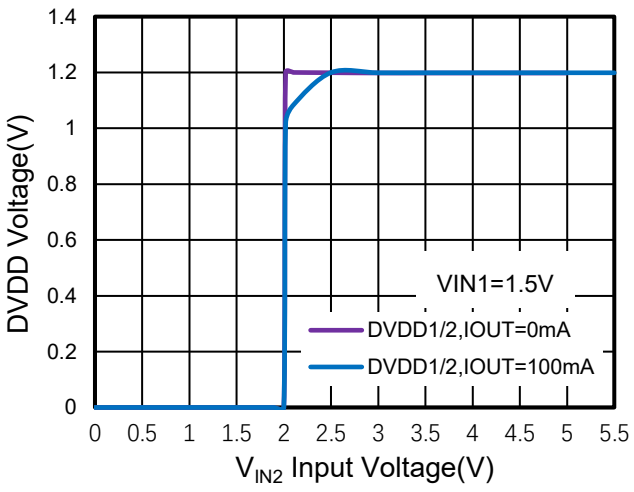


Figure 8 DVDD Voltage vs. Input Voltage

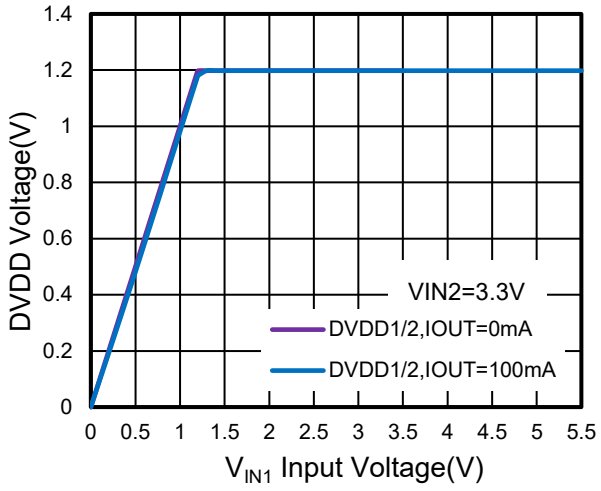


Figure 9 DVDD Voltage vs. Input Voltage

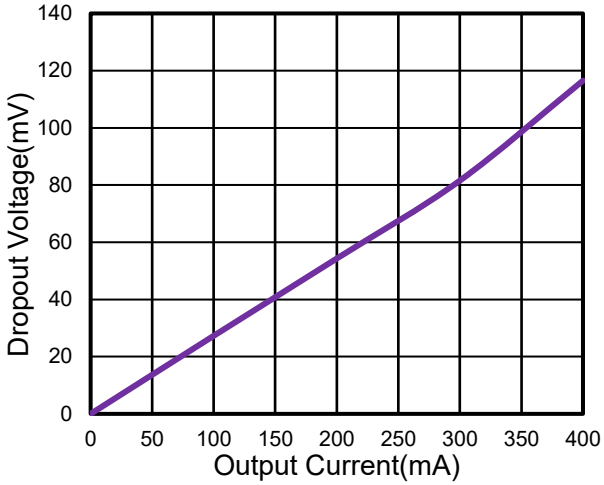


Figure 10 AVDD1 Dropout Voltage vs. Output Current

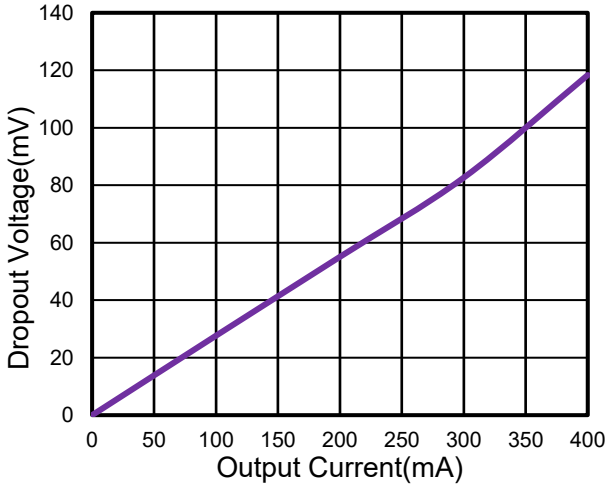


Figure 11 AVDD2 Dropout Voltage vs. Output Current

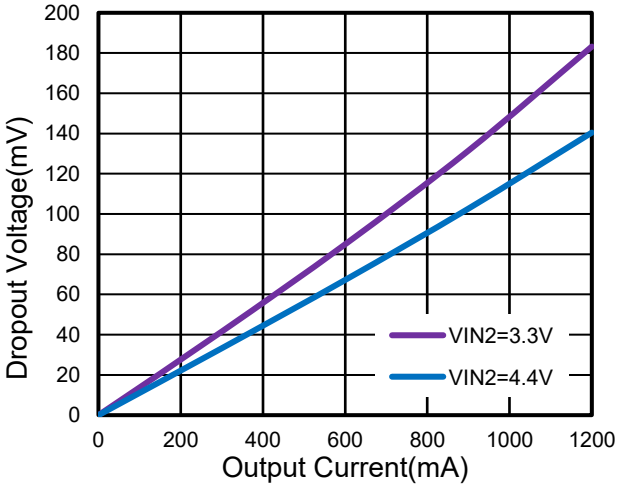


Figure 12 DVDD1 Dropout Voltage vs. Output Current

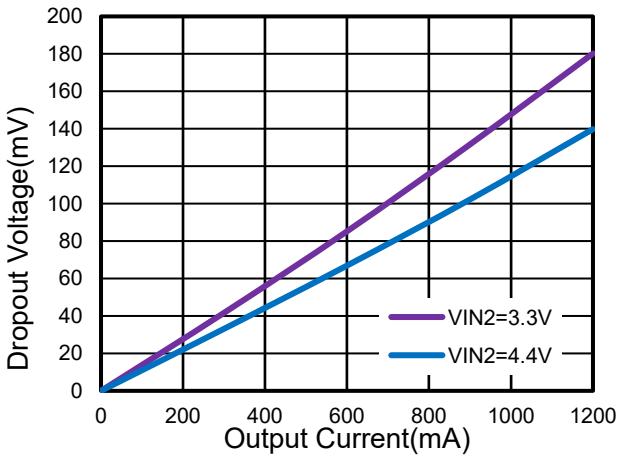


Figure 13 DVDD2 Dropout Voltage vs. Output Current

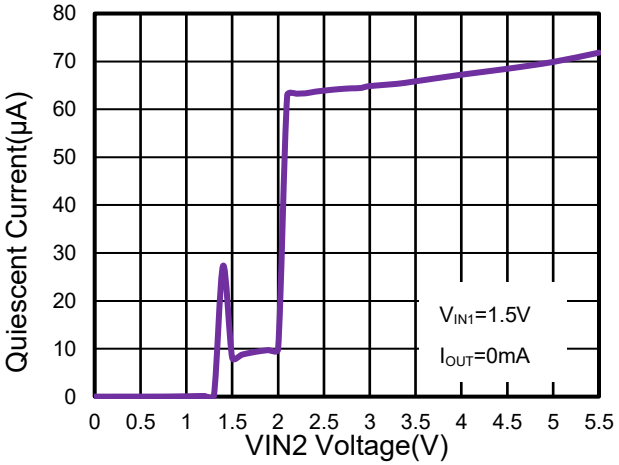


Figure 14 Quiescent Current vs. VIN2 Voltage

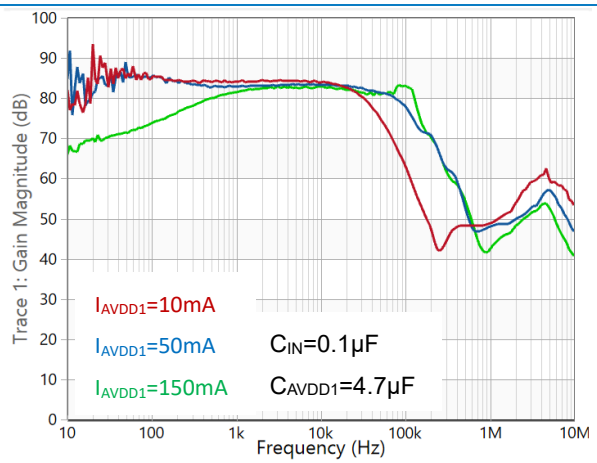


Figure 15 Ripple Rejection vs. Frequency (AVDD1, V_{IN1}=1.35V, V_{IN2}=4.4V+0.2V_{PP})

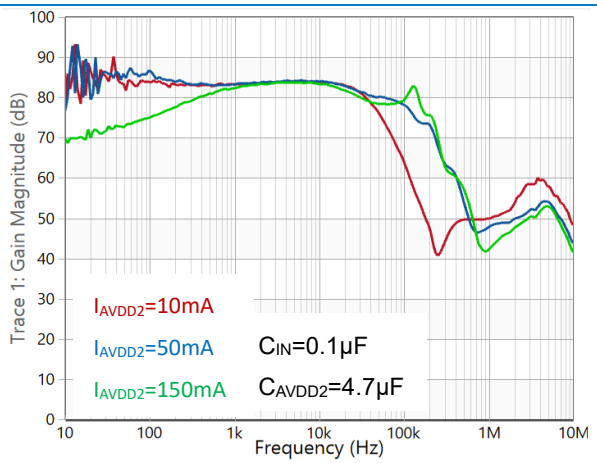


Figure 16 Ripple Rejection vs. Frequency (AVDD2, V_{IN1}=1.35V, V_{IN2}=4.4V+0.2V_{PP})

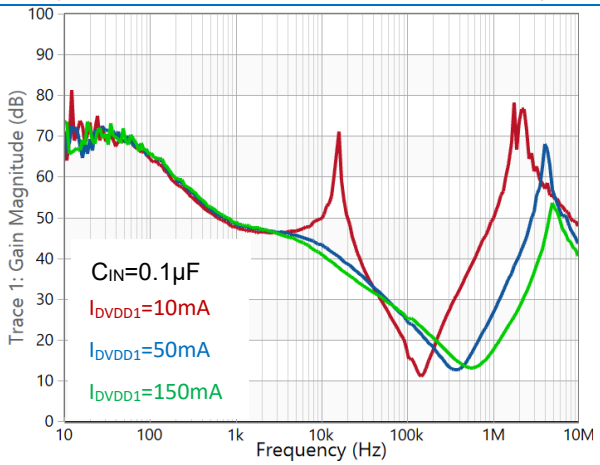


Figure 17 Ripple Rejection vs. Frequency (DVDD1, V_{IN1}=1.35V, V_{IN2}=4.4V+0.2V_{PP})

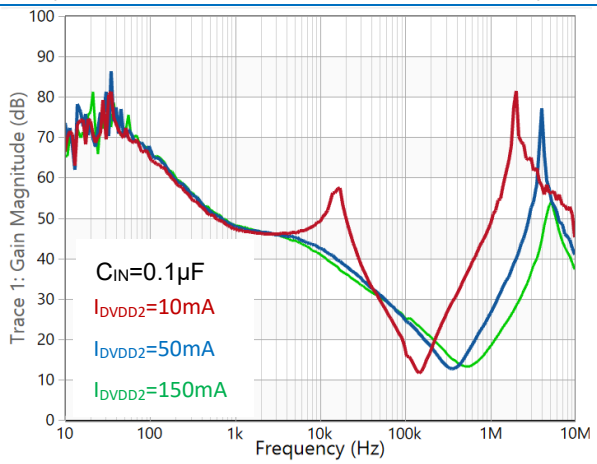


Figure 18 Ripple Rejection vs. Frequency (DVDD2, V_{IN1}=1.35V, V_{IN2}=4.4V+0.2V_{PP})

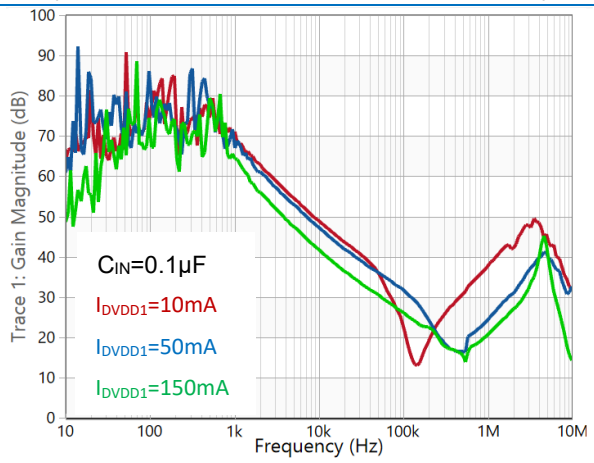


Figure 19 Ripple Rejection vs. Frequency (DVDD1, V_{IN1}=1.35V+0.1V_{PP}, V_{IN2}=4.4V)

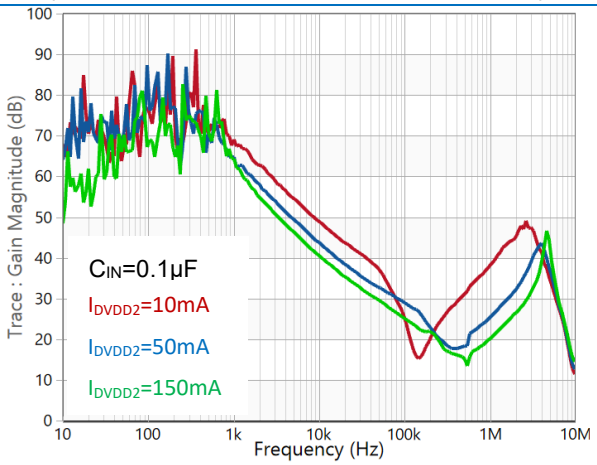


Figure 20 Ripple Rejection vs. Frequency (DVDD2, V_{IN1}=1.35V+0.1V_{PP}, V_{IN2}=4.4V)

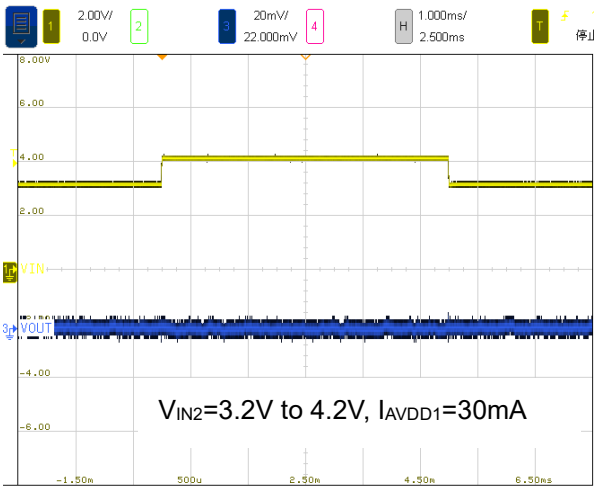


Figure 21 AVDD1, Line Transient
(V_{IN1}=1.35V, tr=tf=1μs)

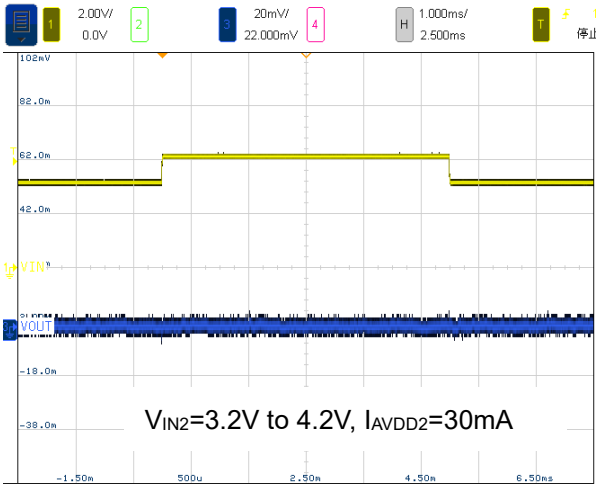


Figure 22 AVDD2, Line Transient
(V_{IN1}=1.35V, tr=tf=1μs)

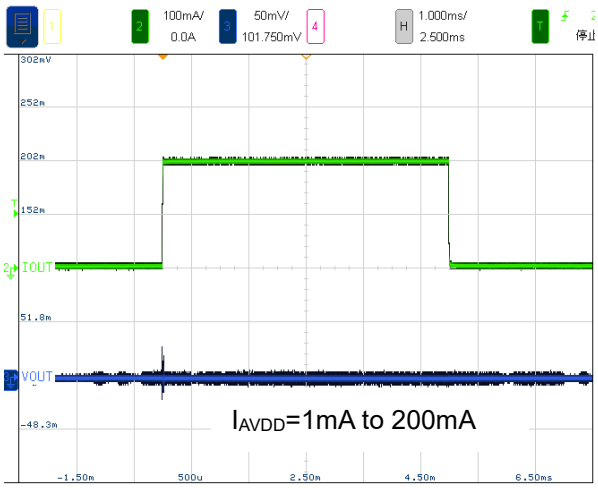


Figure 23 AVDD, Load Transient
(V_{IN1}=1.35V, V_{IN2}=3.3V, tr=tf=1μs)

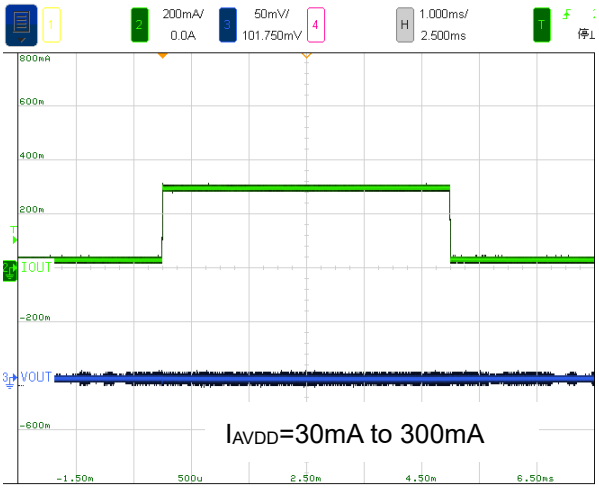


Figure 24 AVDD, Load Transient
(V_{IN1}=1.35V, V_{IN2}=3.3V, tr=tf=1μs)

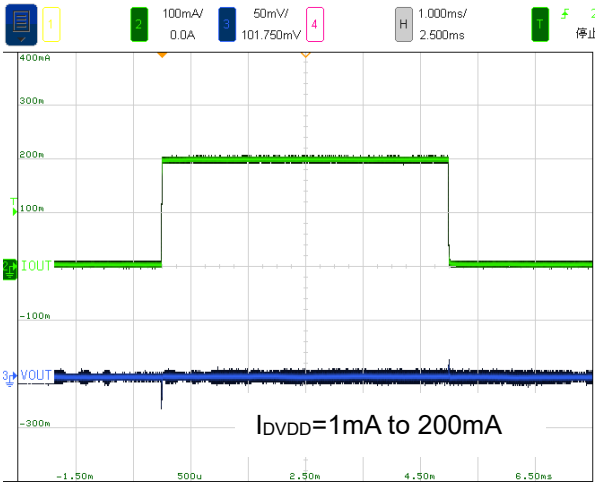


Figure 25 DVDD, Load Transient
(V_{IN1}=1.35V, V_{IN2}=3.3V, tr=tf=1μs)

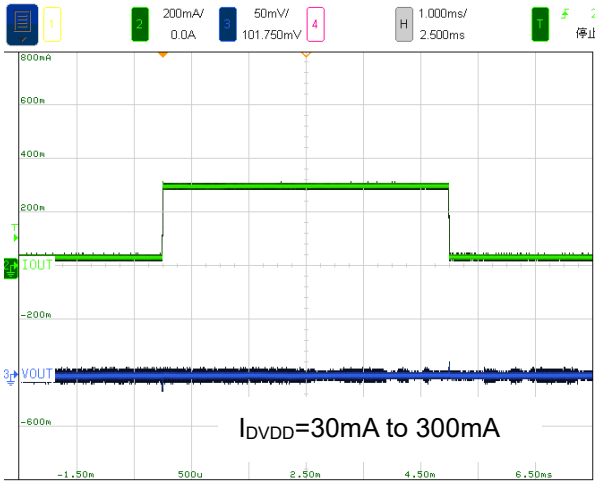


Figure 26 DVDD, Load Transient
(V_{IN1}=1.35V, V_{IN2}=3.3V, tr=tf=1μs)

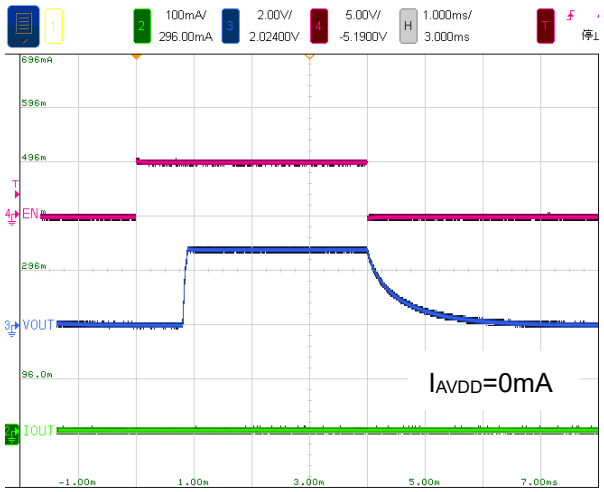


Figure 27 AVDD, Turn-on/off by EN

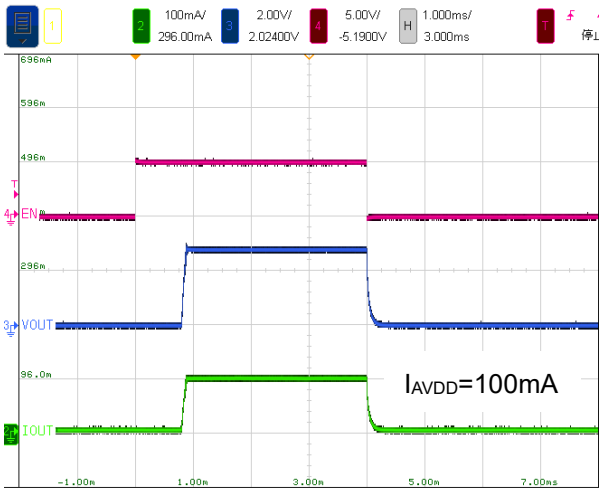


Figure 28 AVDD, Turn-on/off by EN

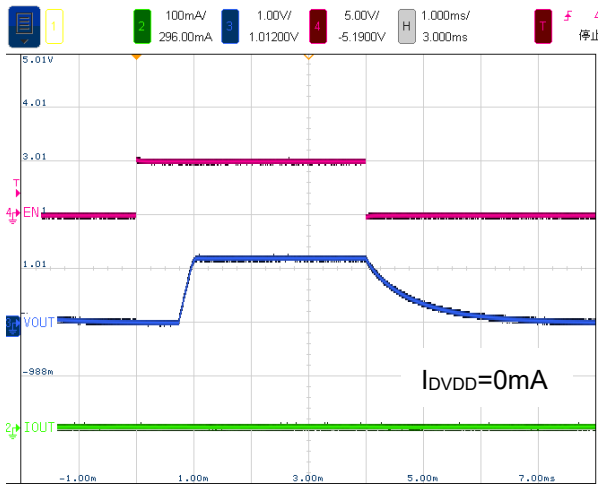


Figure 29 DVDD, Turn-on/off by EN

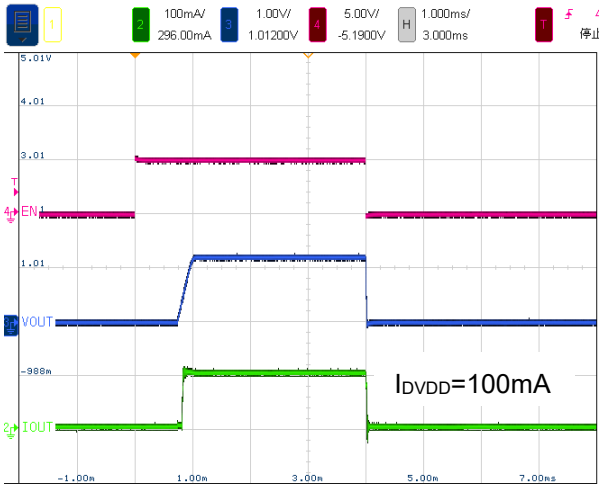


Figure 30 DVDD, Turn-on/off by EN

12. Function Description

12.1 Overview

WR1241 has 4 LDO regulators. Power up/down of each regulator can be controlled by the following three ways.

- Hardware Default On/Off.
- Individual Enable Register On/Off Via I²C.
- Programmable Power Up/Down Via I²C.

Hardware Default On/Off

External EN pin toggles from low to high. It will force 4 LDO regulators powered up, of which output voltages are default voltages. Turn-on delay time is defined as the interval between the assertion of LDO output to the start of its ramp, and soft-start time means the time during soft-start ramp. When external EN pin is high, the WR1241 can ACK data from I²C and update registers but cannot power down LDOs and modify output voltages. Meanwhile, host can set enable control register to startup state, which will avoid LDO regulators powering down when external EN pin toggling from high to low.

Individual Enable Register On/Off

The startup and shutdown of DVDD1/2 and AVDD1/2 channels can be controlled by the Individual Enable Control Register, DVDD1/2_EN and AVDD1/2_EN bits, only if DVDD1/2_SEQ[3:0] and AVDD1/2_SEQ[3:0] bits set to ‘x000’. Before outputting, the user can modify voltage level of each channel through output voltage level definition registers.

Programmable Power Up/Down

The WR1241 has 7 time slots to which each regulator can be assigned. Whichever regulator is assigned to the slot by setting its sequence number not equal to ‘x000’, the system can be powered up by setting SEQ_CTRL bit to ‘1’. Then, SEQ_ON flips to high, and SEQ_COUNT[2:0] starts incrementing from 0 (‘000’) to 7 (‘111’). If LDO’s sequence number is smaller than or equal to current SEQ_COUNT[2:0], this LDO will power up immediately. If SEQ_ON flips to low by setting SEQ_CTRL bit to ‘0’, SEQ_COUNT[2:0] decrements from 7 (‘111’) to 0 (‘000’). The LDO will power off if its sequence number is larger than current SEQ_COUNT[2:0]. Besides, slot can be configured by SEQ_SPEED bits, which will take effect on the present slot if current slot time is less than the set value. Otherwise, SEQ_COUNT[2:0] will count up or down according to SEQ_ON bit or stop at the end. It is recommended to use the same power up method to shut down specified LDOs.

For example, the power-up/down sequences as below Figure 31 and Figure 32 respectively for the four outputs of WR1241 once ‘0001” is assigned to DVDD1_SEQ[3:0] as slot1 and ‘0010” to DVDD2_SEQ[7:4] as slot2 for DVDDx Sequence Control Register (Address 0x0A), ‘0011” to AVDD1_SEQ[3:0] as slot3 and ‘0100” to AVDD2_SEQ[3:0] as slot4 for AVDDx Sequence Control Register (Address 0x0B).

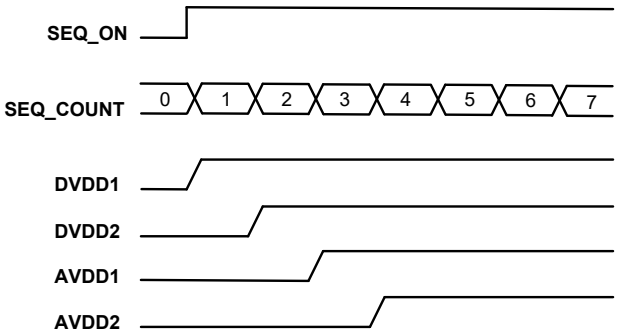


Figure 31 Power-up Sequence

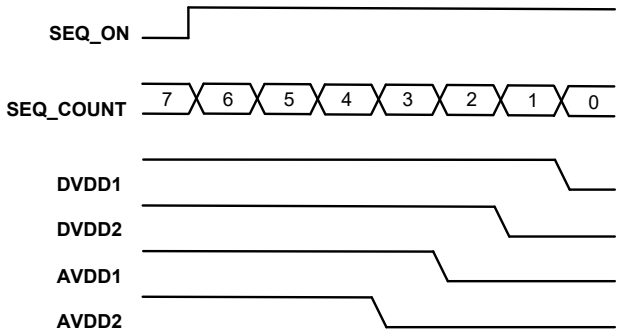
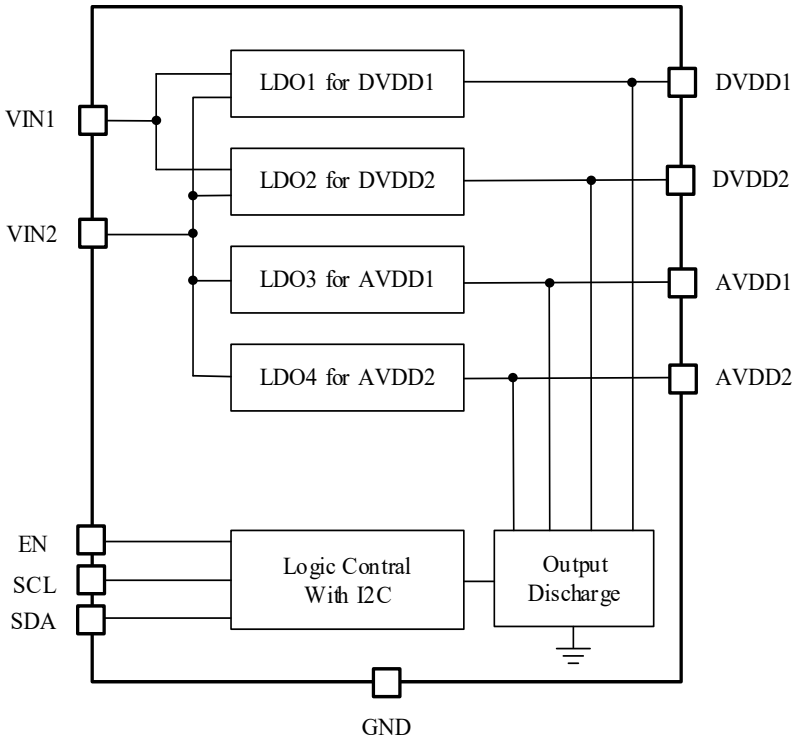


Figure 32 Power-down Sequence

12.2 Block Diagram



12.3 Feature Description

12.3.1 Output Voltage Accuracy

WR1241 has an output voltage accuracy of 2%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, considering differences between manufacturing lots.

12.3.2 Dropout Voltage (V_{DROP})

WR1241 is a low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the minimum of (V_{IN}-V_{OUT}) at the rated maximum output current where V_{OUT} is the minimum of $V_{OUT(NOM)}$. When the input voltage is below $V_{OUT(NOM)}$ plus V_{DO}, the output voltage varies with the input voltage.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS\ (ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for those current scales accordingly. The $R_{DS\ (ON)}$ is calculated by following equation.

$$R_{DS(ON)} = V_{DROP}/I_{OUT}$$

12.3.3 Power Supply Rejection Ratio (PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$PSRR = 20 \times \lg\left(\frac{Ripple(V_{IN})}{Ripple(V_{OUT})}\right)$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

12.3.4 Noise

LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics; external noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimizing noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

12.3.5 Foldback Current Limit (I_{CL})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at I_{MAX}, and the output voltage will be reduced to I_{MAX}*R_{LOAD}.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{MAX}. The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to I_{FB}*R_{LOAD}. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

12.3.6 Thermal Protection

WR1241 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 155°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 125°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

WR1241's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR1241 into a thermal shutdown state will reduce the reliability of the device.

13. I^2C interface

WR1241 utilizes an I^2C interface to write / read internal registers. It supports 100Kbps standard mode, 400Kbps fast mode and 1Mbps fast mode plus. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I^2C, 1kΩ is recommended for 1MHz I^2C. The voltage from 1.8V to 3.3V is allowed for the I^2C interface. Additionally, the I^2C device supports continuous reading and writing operations.

I2C Slave Address of WR1241: 0x28

Bit Types:

R: Read only

R/W: Read/Write

13.1 I²C Serial Data Bus

The WR1241 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The WR1241 operates as a slave to the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The WR1241 operates in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The following bus protocol has been defined Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

13.2 Device Address

The I²C device address is 0x28 which is 7-bit (A7-A1), followed by the R/W bit A0 (Read=1/Write=0). Set A0 to “0” for writing and “1” for reading.

A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	W/R

13.3 I²C Start/Stop

I²C Start: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

I²C Stop: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

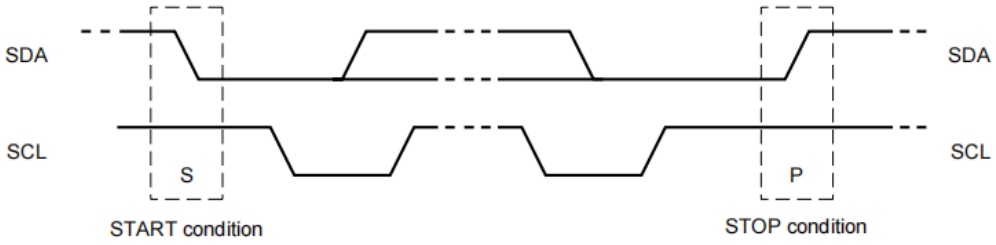


Figure 33 I²C Start/Stop

13.4 Date Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited and are determined by the master device. The information is transferred byte-wise, and each receiver acknowledges with a ninth bit.

13.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be considered. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

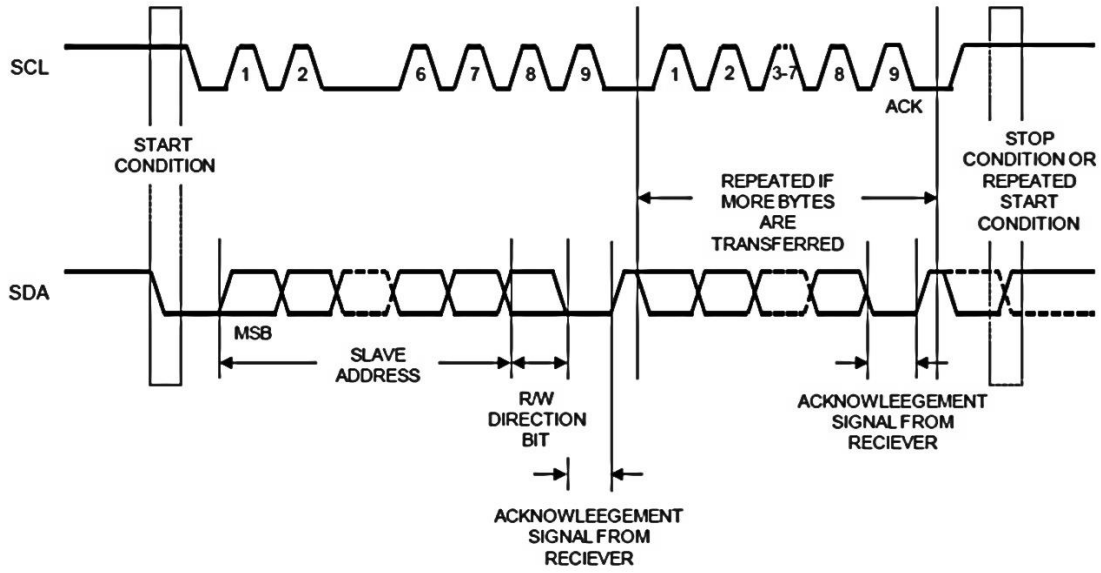


Figure 34 I²C Acknowledge

13.6 Register Maps

Add.	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Init
0x00	CHIP_ID	R	CHIP_ID								0x00
0x19	CHIP_ID2	R	CHIP_ID2								0x04
0x01	CLMTCR	R/W	AVDD2_CLMT		AVDD1_CLMT		DVDD2_CLMT		DVDD1_CLMT		0x00
0x02	DISCR	R/W	DISCHG_MD				AVDD2_DISCHG	AVDD1_DISCHG	DVDD2_DISCHG	DVDD1_DISCHG	0x00
0x03	DVDD1_VOUT	R/W	DVDD1_VOUT								0x64
0x04	DVDD2_VOUT	R/W	DVDD2_VOUT								0x64
0x05	AVDD1_VOUT	R/W	AVDD1_VOUT								0x80
0x06	AVDD2_VOUT	R/W	AVDD2_VOUT								0x80
0x0A	DVDD_SEQ	R/W	DVDD2_SEQ				DVDD1_SEQ				0x00
0x0B	AVDD_SEQ	R/W	AVDD2_SEQ				AVDD1_SEQ				0x00
0x0E	ENCR	R/W					AVDD2_EN	AVDD1_EN	DVDD2_EN	DVDD1_EN	0x00
0x0F	SEQCR	R/W	SEQ_SPEED			SEQ_CTRL	SEQ_ON	SEQ_COUNT			0x00

13.7 Register Description

CHIP_ID: Chip ID (Address 0x00)

Bit	Symbol	R/W	Description	Default
7:0	CHIP ID	R	Indicates the device ID	0x00

CHIP_ID2: Chip ID (Address 0x19)

Bit	Symbol	R/W	Description	Default
7:0	CHIP ID2	R	Indicates the device ID	0x04

CLMTCR: Current Limit Control Register (Address 0x01)

Bit	Symbol	R/W	Description	Default
7:6	AVDD2_CLMT	R/W	AVDD2 current limit control 00: I_{CL_TYP} =480mA; (Default) 01: I_{CL_TYP} +140mA; 10: I_{CL_TYP} +280mA; 11: I_{CL_TYP} +420mA.	00
5:4	AVDD1_CLMT	R/W	AVDD2 current limit control 00: I_{CL_TYP} =480mA; (Default) 01: I_{CL_TYP} +140mA; 10: I_{CL_TYP} +280mA; 11: I_{CL_TYP} +420mA.	00
3:2	DVDD2_CLMT	R/W	DVDD2 current limit control 00: I_{CL_TYP} =1300mA; (Default) 01: I_{CL_TYP} +140mA; 10: I_{CL_TYP} +280mA; 11: I_{CL_TYP} +420mA.	00
1:0	DVDD1_CLMT	R/W	DVDD1 current limit control 00: I_{CL_TYP} =1300mA; (Default) 01: I_{CL_TYP} +140mA; 10: I_{CL_TYP} +280mA; 11: I_{CL_TYP} +420mA.	00

DISCR: Discharge Control Register (Address 0x02)

Bit	Symbol	R/W	Description	Default
7	DISCHG_MD	R/W	Discharge mode control 0: Auto mode, all LDOs discharge function is enable; 1: Manuel mode, discharge function controlled by DVDDx_DISCHG & AVDDx_DISCHG.	0
6:4	RESERVED	R	Reserved	000
3	AVDD2_DISCHG	R/W	Discharge function enable of AVDD2 0: Disable; 1: Enable.	0
2	AVDD1_DISCHG	R/W	Discharge function enable of AVDD1 0: Disable; 1: Enable.	0
1	DVDD2_DISCHG	R/W	Discharge function enable of DVDD2 0: Disable; 1: Enable.	0
0	DVDD1_DISCHG	R/W	Discharge function enable of DVDD1 0: Disable; 1: Enable.	0

DVDD1_VOUT: DVDD1 Output Voltage Control Register (Address 0x03)

Bit	Symbol	R/W	Description	Default
7:0	DVDD1_VOUT	R/W	DVDD1 output voltage control VOUT1=0.6V+DVDD1_VOUT[7:0]*0.006V 0x00: 0.600V 0x01: 0.606V 0x02: 0.612V … 0x63: 1.194V 0x64: 1.200V (Default) 0x65: 1.206V … 0xFF: 2.130V	0x64

DVDD2_VOUT: DVDD2 Output Voltage Control Register (Address 0x04)

Bit	Symbol	R/W	Description	Default
7:0	DVDD2_VOUT	R/W	DVDD2 output voltage control VOUT2=0.6V+DVDD2_VOUT[7:0]*0.006V 0x00: 0.600V 0x01: 0.606V 0x02: 0.612V … 0x63: 1.194V 0x64: 1.200V (Default) 0x65: 1.206V … 0xFF: 2.130V	0x64

AVDD1_VOUT: AVDD1 Output Voltage Control Register (Address 0x05)

Bit	Symbol	R/W	Description	Default
7:0	AVDD1_VOUT	R/W	AVDD1 output voltage control VOUT1=1.2V+AVDD1_VOUT[7:0]*0.0125V 0x00: 1.2000V 0x01: 1.2125V 0x02: 1.2250V … 0x7F: 2.7875V 0x80: 2.8000V (Default) 0x81: 2.8125V … 0xFF: 4.3875V	0x80

AVDD2_VOUT: AVDD2 Output Voltage Control Register (Address 0x06)

Bit	Symbol	R/W	Description	Default
7:0	AVDD2_VOUT	R/W	AVDD2 output voltage control VOUT2=1.2V+AVDD2_VOUT[7:0]*0.0125V 0x00: 1.2000V 0x01: 1.2125V 0x02: 1.2250V … 0x7F: 2.7875V 0x80: 2.8000V (Default) 0x81: 2.8125V … 0xFF: 4.3875V	0x80

DVDD_SEQ: DVDDx Sequence Control Register (Address 0x0A)

Bit	Symbol	R/W	Description	Default
7:4	DVDD2_SEQ	R/W	DVDD2 sequence slot set 0000: disable sequence mode; x001: set sequence slot is 1; x010: set sequence slot is 2; x011: set sequence slot is 3; x100: set sequence slot is 4; x101: set sequence slot is 5; x110: set sequence slot is 6; x111: set sequence slot is 7.	0000
3:0	DVDD1_SEQ	R/W	DVDD1 sequence slot set 0000: disable sequence mode; x001: set sequence slot is 1; x010: set sequence slot is 2; x011: set sequence slot is 3; x100: set sequence slot is 4; x101: set sequence slot is 5; x110: set sequence slot is 6; x111: set sequence slot is 7.	0000

AVDD_SEQ: AVDDx Sequence Control Register (Address 0x0B)

Bit	Symbol	R/W	Description	Default
7:4	AVDD2_SEQ	R/W	AVDD2 sequence slot set 0000: disable sequence mode; x001: set sequence slot is 1; x010: set sequence slot is 2; x011: set sequence slot is 3; x100: set sequence slot is 4; x101: set sequence slot is 5; x110: set sequence slot is 6; x111: set sequence slot is 7.	0000
3:0	AVDD1_SEQ	R/W	AVDD1 sequence slot set 0000: disable sequence mode; x001: set sequence slot is 1; x010: set sequence slot is 2; x011: set sequence slot is 3; x100: set sequence slot is 4; x101: set sequence slot is 5; x110: set sequence slot is 6; x111: set sequence slot is 7.	0000

ENCR: Individual Enable Control Register (Address 0x0E)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3	AVDD2_EN	R/W	AVDD2 enable control 0: Disable; 1: Enable.	0
2	AVDD1_EN	R/W	AVDD1 enable control 0: Disable; 1: Enable.	0
1	DVDD2_EN	R/W	DVDD2 enable control 0: Disable; 1: Enable.	0
0	DVDD1_EN	R/W	DVDD1 enable control 0: Disable; 1: Enable.	0

SEQCR: Sequence Control Register (Address 0x0F)

Bit	Symbol	R/W	Description	Default
7:6	SEQ_SPEED	R/W	The seq_count increment period in sequence mode 00: 2.00ms; 01: 1.00ms; 10: 0.50ms; 11: 0.25ms.	00
5	RESERVED	R	Reserved	0
4	SEQ_CTRL	R/W	Sequence control when AVDDx/DVDDx slot isn't 0 0: Shutdown; 1: Power up.	0
3	SEQ_ON	R	The indication of sequence activation 0: Shutdown; 1: Power up.	0
2:0	SEQ_COUNT	R	The indication of the SEQ slot number at moment 000: No LDO slots active; 001: slots 1 active; 010: slots 2 active; 011: slots 3 active; 100: slots 4 active; 101: slots 5 active; 110: slots 6 active; 111: slots 7 active, and stop counting.	000

14. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

14.1 Application Information

WR1241 is a 4-channel LDO PMIC for camera applications including 2-Ch DVDD, 2-Ch AVDD. With 400kHz high speed I^2C interface, the function setting is flexible such as power sequence, output voltage, output discharge. The chip enables control supporting EN pin control and I^2C control. This section discusses how best to use this device in practical applications.

14.2 Capacitor Recommendation

WR1241 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN} and V_{OUT} pins to increase its stability. Multilayer ceramic capacitors are recommended. These capacitors also have limitations, and ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials have relatively good capacitance stability at different temperatures. WR1241 is designed to use ceramic capacitors of 4.7μF or larger at the input, 2.2μF or larger for DVDD1/2, and 1.0μF or larger for AVDD1/2. Place C_{IN} and C_{OUT} as close to the IN and OUT pins as possible to minimize trace inductance from the capacitor to the device.

14.3 Power Dissipation (P_D)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

P_D can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance ($R_{\theta JA}$) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

The thermal resistance ($R_{\theta JA}$) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance.

The module names are listed in the following table.

Name	Package	Evaluation Module
WR1241	DFN2×2-10L	WR1241_EVB

15.1 Typical Application Circuits

This section discusses the application of WR1241 in the circuit. The following figure shows the schematic of the application circuit.

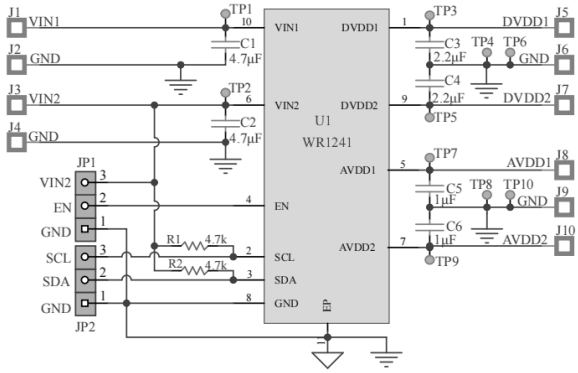


Figure 35 Schematic for EVB

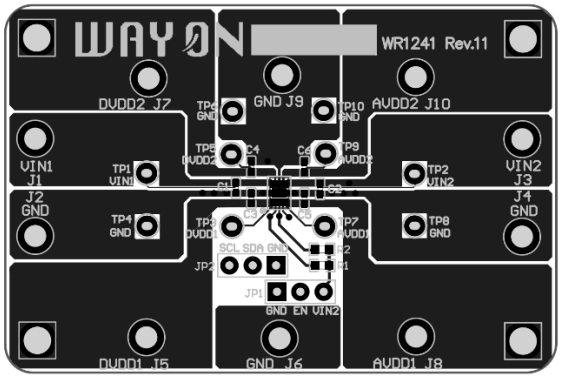


Figure 36 PCB Layout for EVB

15.2 Layout of Typical Application Circuits

Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. A 4.7μF or larger input capacitor (C_{IN}) is recommended to VIN to minimize the effect of resistance and inductance between the source and the LDO input. A 2.2μF or larger output capacitor (C_{OUT}) is recommended for DVDD1/2. A 1.0μF or larger output capacitor (C_{OUT}) is recommended for AVDD1/2. Connect the ground sides of C_{IN} and C_{OUT} with LDO ground pins as close as possible through a wide copper surface. Through-holes and long wires may seriously affect system performance and are not recommended.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

16. Naming Conventions

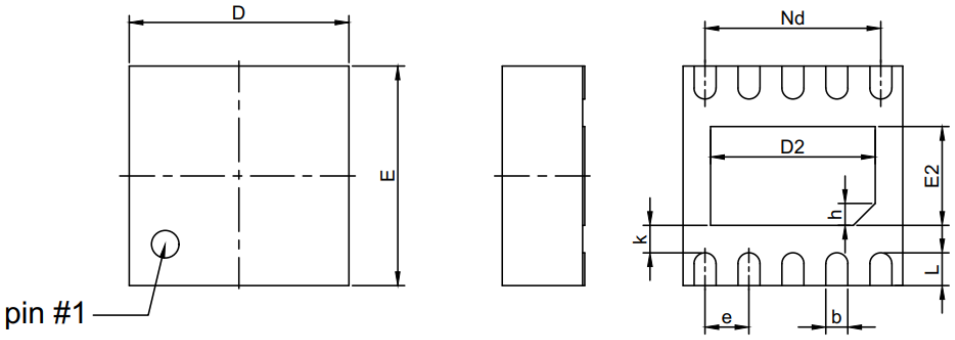
WR AA BB-CC DDD E
WR: WAYON Regulator
AA: 12 - Output Current, 1.2A
BB: Serial number
CC: Output Voltage/AD-Output Voltage, Adjustable Voltage
DDD: Package –FYA: DFN2×2-10L
E: R-Reel

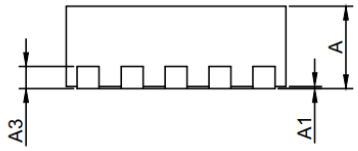
17. Electrostatic Discharge Warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

18. Package Information

DFN2×2-10L





SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.10	-	0.25
b	0.15	0.20	0.25
D	1.90	2.00	2.10
D2	1.30	1.50	1.60
E	1.90	2.00	2.10
E2	0.70	0.90	1.00
e	0.40BSC		
Nd	1.60BSC		
L	0.20	0.30	0.40
k	0.20	-	-
h	0.20REF		

19. Ordering Information

PART NUMBER	Package	Packing Quantity	Marking*
WR1241-ADFYAR	DFN2×2-10L	3k/Reel	1241 XXXX

* XXXX is variable.

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For additional information, please contact your local Sales Representative.
WAYON® is registered trademark of Wayon Corporation.

Specifications are subject to change without notice.
The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

Product Specification Statement

- The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.
- The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. WAYON shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and WAYON assumes no responsibility for the application of the product.
- WAYON strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, WAYON cannot guarantee that the information provided in the product specification is entirely accurate and error-free. WAYON shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications. WAYON reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with WAYON to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult WAYON in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.
- Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.
- The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. WAYON shall assume no responsibility for any consequences resulting from such usage.
- Users should also comply with relevant laws, regulations, policies, and standards when using the product specification. Users are responsible for the risks and liabilities arising from the use of the product specification and must ensure that it is not used for illegal purposes. Additionally, users should respect the intellectual property rights related to the product specification and refrain from infringing upon any third-party legal rights. WAYON shall assume no responsibility for any disputes or controversies arising from the above-mentioned issues in any form.